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64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4 RAM) 82S25

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

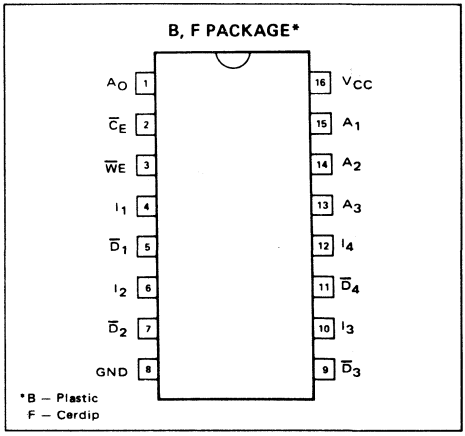
The 82S25 is a 64-bit, Schottky clamped TTL, Read-Write Random Access Memory ideal for use in scratch pad and high-speed buffer memory applications.

The 82S25 is a fully decoded memory array organized as 16 words of 4 bits each, with separate input and output lines. It features PNP inputs, one chip enable line, and open collector outputs for ease of memory expansion.

The outputs of the 82S25 assume a logic "1" state during write. This allows both memory inputs and outputs to share a common bus for minimizing interconnections, and more effective utilization of common I/O circuitry.

The 82S25 is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S25, B or F. For the military temperature range (−55°C to +125°C) specify S82S25, F only.

PIN CONFIGURATION



FEATURES

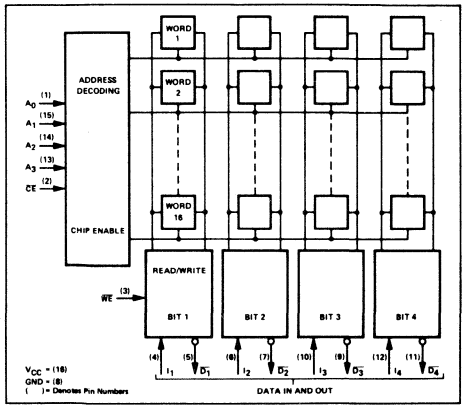
- ORGANIZATION — 16 X 4
- ADDRESS ACCESS TIME:
  S82S25 — 60ns, MAXIMUM
  N82S25 — 50ns, MAXIMUM
- WRITE CYCLE TIME:
  S82S25 — 50ns, MAXIMUM
  N82S25 — 35ns, MAXIMUM
- POWER DISSIPATION — 6.25mW/BIT, TYPICAL
- INPUT LOADING:
  S82S25 — (−150μA) MAXIMUM
  N82S25 — (−100μA) MAXIMUM
- OUTPUT BLANKING DURING WRITE
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- 16 PIN CERAMIC DIP

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	In	$\overline{Dn}$
Read	0	1	X	Complement of data stored
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

X = Don't care.

BLOCK DIAGRAM



APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
PUSH DOWN STACKS
CONTROL STORE

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S25)	0° to +75°	°C
	(S82S25)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S25 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S25 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S25[1,2,3]			N82S25[1,2,3]			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
I_{IL}	"0" Input Current	V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			25			10	μA
V_{IL}	"0" Level Input Voltage	V_{CC} = MIN			.80			.85	V
V_{IH}	"1" Level Input Voltage	V_{CC} = MAX	2.0			2.0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −12mA, V_{CC} = MIN (Note 6)		−1.0	−1.5		−1.0	−1.5	V
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA, V_{CC} = MIN (Notes 4, 5)		0.35	0.5		0.35	0.45	V
C_{IN}	Input Capacitance	V_{IH} = 2.0V, V_{CC} = 5.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V, $\overline{CE}$ = "1"		8			8		pF
I_{CC}	Power Supply Current	(Note 5)		80	120		80	105	mA
I_{OLK}	Output Leakage Current	$\overline{CE}$ = "1", V_{OUT} = 5.5V, V_{CC} = MIN		<1	100		<1.0	100	μA

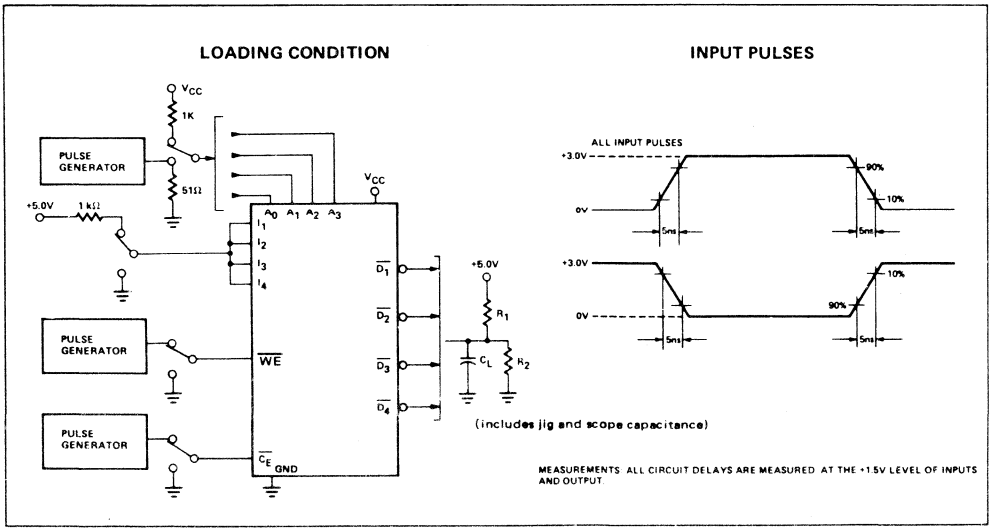
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Positive current is defined as into the terminal referenced.
3. Positive logic definition: "1" = HIGH ≈ +5.0V; "0" = LOW ≈ GRD.
4. Output sink current is supplied through a resistor to V_{CC}.
5. All sense outputs in "0" state.
6. Test each input one at a time.
7. To guarantee a WRITE into the slowest bit.
8. Typical values are at V_{CC} = +5.0V and T_A = +25°C.

SWITCHING CHARACTERISTICS

S82S25 $-55°C \leqslant T_A \leqslant +125°C$, $4.5V \leqslant V_{CC} \leqslant 5.5V$
N82S25 $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	S82S25			N82S25			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
Propagation Delays									
T_{AA}	Address Access Time			35	60		35	50	ns
T_{CE}	Chip Enable Access Time			20	35		20	35	ns
T_{CD}	Chip Enable Output Disable Time			20	35		20	35	ns
T_{WD}	Write Enable to Output Disable Time			20	30		20	25	ns
T_{WR}	Write Recovery Time			35	60		35	50	ns
Write Set-up Times		$R_1 = 270\Omega$ $R_2 = 600\Omega$							
T_{WSA}	Address to Write Enable	$C_L = 30pF$	10	-8		0	-8		ns
T_{WSD}	Data In to Write Enable		25	5		20	5		ns
T_{WSC}	$\overline{CE}$ to Write Enable		0	-5		0	-5		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		10	-3		5	-3		ns
T_{WHC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 7)		30	18		30	18		ns

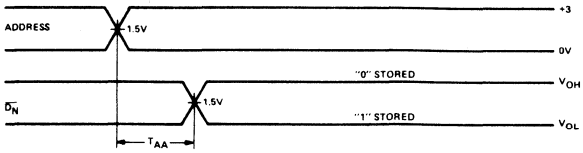
AC TEST LOAD AND WAVEFORMS



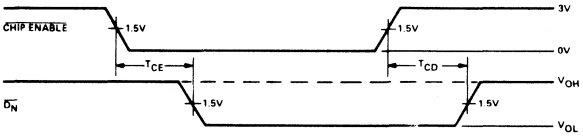
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

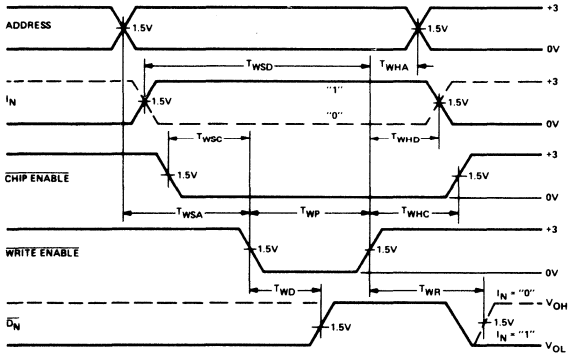
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid – not as shown.)

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

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64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4 RAM) | 3101A

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 3101A is a 64-bit, Schottky clamped TTL, Read-Write Random Access Memory ideal for use in scratch pad and high-speed buffer memory applications.

The 3101A is a fully decoded memory array organized as 16 words of 4 bits each, with separate input and output lines. It features PNP inputs, one chip enable line, and open collector outputs for ease of memory expansion.

The outputs of the 3101A assume a logic "1" state during write. This allows both memory inputs and outputs to share a common bus for minimizing interconnections, and more effective utilization of common I/O circuitry.

The 3101A is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N3101A, B or F. For the military temperature range (−55°C to +125°C) specify S3101A, F only.

FEATURES

- ORGANIZATION – 16 X 4
- ADDRESS ACCESS TIME:
  S3101A – 50ns, MAXIMUM
  N3101A – 35ns, MAXIMUM
- WRITE CYCLE TIME:
  S3101A – 25ns, MAXIMUM
  N3101A – 25ns, MAXIMUM
- POWER DISSIPATION – 6.25mW/BIT, TYPICAL
- INPUT LOADING:
  S3101A – (−150μA) MAXIMUM
  N3101A – (−100μA) MAXIMUM
- OUTPUT BLANKING DURING WRITE
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- 16 PIN CERAMIC DIP

APPLICATIONS

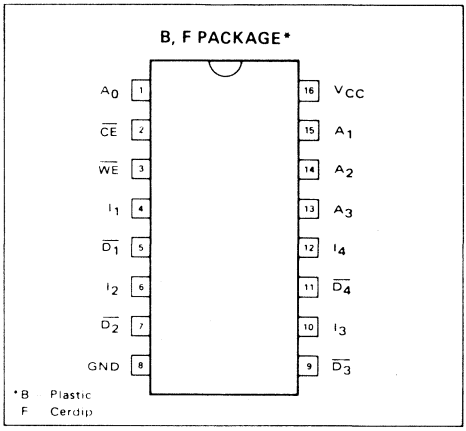
SCRATCH PAD MEMORY

BUFFER MEMORY

PUSH DOWN STACKS

CONTROL STORE

PIN CONFIGURATION

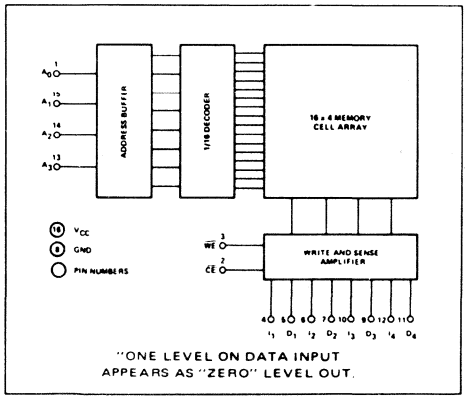


TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	$\overline{D}_N$
READ	0	1	X	Complement of Data Stored
WRITE "0"	0	0	0	1
WRITE "1"	0	0	1	1
DISABLED	1	X	X	1

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range		
	(N3101A)	0° to +75°	°C
	(S3101A)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S3101A $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N3101A $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S3101A[1,2,3]			N3101A[1,2,3]			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
I_{IL}	"0" Input Current	$V_{IN} = 0.45V$		−10	−150		−10	−100	μA
I_{IH}	"1" Input Current	$V_{IN} = 5.5V$			25			10	μA
V_{IL}	"0" Level Input Voltage	V_{CC} = MIN			.80			.85	V
V_{IH}	"1" Level Input Voltage	V_{CC} = MAX	2.0			2.0			V
V_{IC}	Input Clamp Voltage	$I_{IN} = -12mA$, V_{CC} = MIN (Note 6)					−1.0	−1.5	V
		$I_{IN} = -18mA$, V_{CC} = MIN (Note 6)		−0.8	−1.2				V
V_{OL}	"0" Output Voltage	$I_{OUT} = 16mA$, V_{CC} = MIN (Notes 4, 5)		0.35	0.5		0.35	0.45	V
C_{IN}	Input Capacitance	$V_{IH} = 2.0V$, $V_{CC} = 5.0V$		5			5		pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0V$, $V_{CC} = 5.0V$, $\overline{CE}$ = "1"		8			8		pF
I_{CC}	Power Supply Current	(Note 5)		80	105		80	105	mA
I_{OLK}	Output Leakage Current	$\overline{CE}$ = "1", $V_{OUT} = 5.5V$, V_{CC} = MIN		<1	100		<1.0	100	μA
		$\overline{CE}$ = "1", $V_{OUT} = 2.4V$, V_{CC} = MIN		<1	40				μA

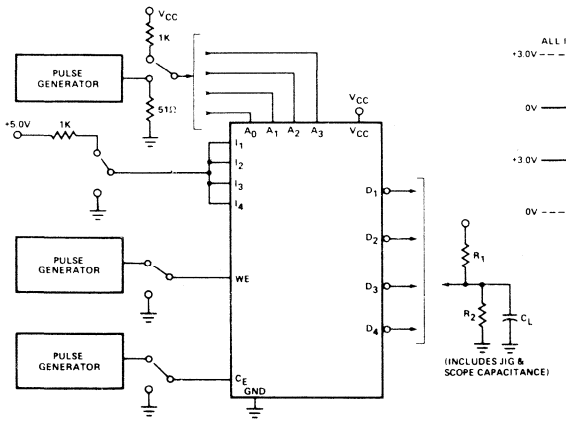
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Positive current is defined as into the terminal referenced.
3. Positive logic definition: "1" = HIGH ≈ +5.0V, "0" = LOW ≈ GRD.
4. Output sink current is supplied through a resistor to V_{CC}.
5. All sense outputs in "0" state.
6. Test each input one at a time.
7. To guarantee a WRITE into the slowest bit.
8. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25°C$.

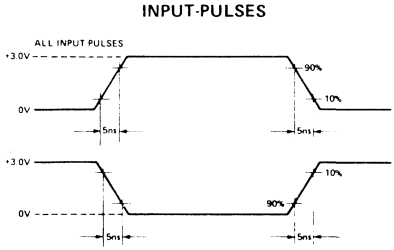
SWITCHING CHARACTERISTICS

S3101A $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, $4.5V \leq V_{CC} \leq 5.5V$
N3101A $0^{\circ}C \leq T_A \leq +75^{\circ}C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S3101A			N3101A			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
Propagation Delays									
T_{AA}	Address Access Time			25	50	10		35	ns
T_{CE}	Chip Enable Access Time			12	25	5		17	ns
T_{CD}	Chip Enable Output Disable Time			12	25	5		17	ns
T_{WD}	Write Enable to Output Disable Time			15	25			20	ns
T_{WR}	Write Recovery Time	$R_1 = 270\Omega$		22	40			35	ns
Write Set-up Times		$R_2 = 600\Omega$							
T_{WSA}	Address to Write Enable	$C_L = 30pF$	0			0	-8		ns
T_{WSD}	Data In to Write Enable		25			20	5		ns
T_{WSC}	$\overline{CE}$ to Write Enable		0			0	-5		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		0			0			ns
T_{WHD}	Data In to Write Enable		0			0	-3		ns
T_{WHC}	$\overline{CE}$ to Write Enable		0			0			ns
T_{WP}	Write Enable Pulse Width (Note 7)		25	18		25	18		ns

AC TEST LOAD AND WAVEFORMS



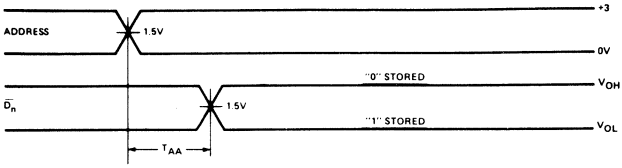


MEASUREMENTS ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT

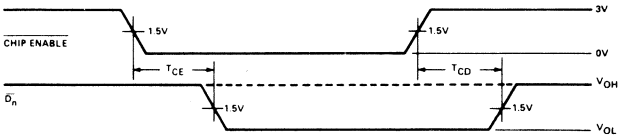
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

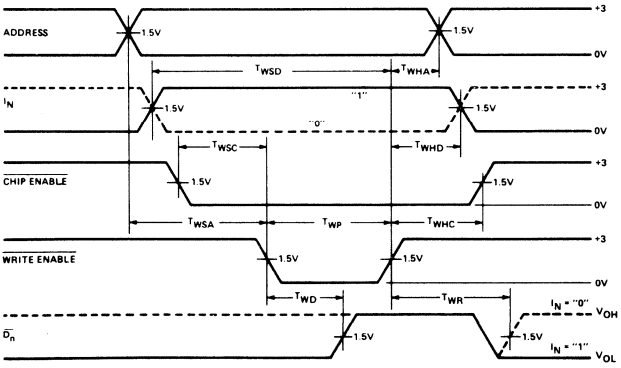
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid—not as shown.)

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

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256-BIT BIPOLAR RAM (256x1 RAM) (82S16 TRI-STATE) (82S17 OPEN COLLECTOR)

82S16 82S17

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S16 and 82S17 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state output options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading to 25μA for a "1" level, and -250μA (S82S16/17) or -100μA (N82S16/17) for a "0" level.

During WRITE operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both 82S16 and 82S17 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S16/17, B or F. For the military temperature range (-55°C to +125°C) specify S82S16/17, F only.

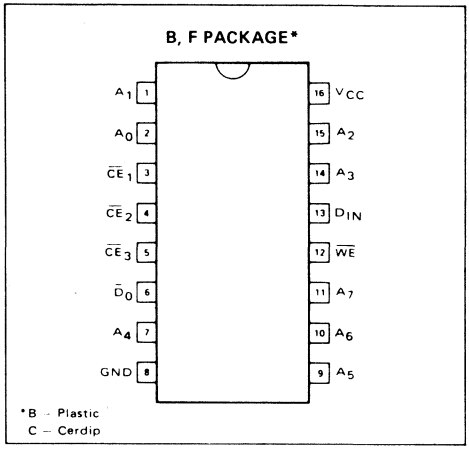
FEATURES

- ORGANIZATION – 256 X 1
- ADDRESS ACCESS TIME:
  S82S16, S82S17 – 70ns, MAXIMUM
  N82S16, N82S17 – 50ns, MAXIMUM
- WRITE CYCLE TIME:
  S82S16, S82S17 – 70ns, MAXIMUM
  N82S16, N82S17 – 55ns, MAXIMUM
- POWER DISSIPATION – 1.5mW/BIT TYPICAL
- INPUT LOADING:
  S82S16, S82S17 – (-250μA) MAXIMUM
  N82S16, N82S17 – (-100μA) MAXIMUM
- OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE
- ON-CHIP ADDRESS DECODING
- 16 PIN CERAMIC DIP
- OUTPUT OPTION:
  TRI-STATE – 82S16
  OPEN COLLECTOR – 82S17

APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

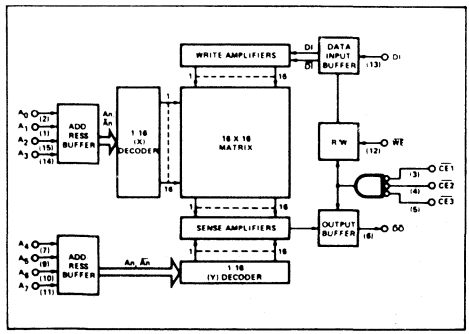


TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82S16	82S17
READ	0	1	X	STORED $\overline{DATA}$	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1	1
WRITE "1"	0	0	1	0	0
DISABLED	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OUT}	High Level Output Voltage (82S17)	+5.5	Vdc
V_O	Off-State Output Voltage (82S16)	+5.5	Vdc
T_A	Operating Temperature Range		
	S82S16/17	−55° to +125°	°C
	N82S16/17	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S16/17 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S16/17 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS		N82S16/17			S82S16/17			UNIT	NOTES
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX		
V_{IH}	High-Level Input Voltage	V_{CC} = MAX		2.0			2.0			V	1
V_{IL}	Low-Level Input Voltage	V_{CC} = MIN				0.85			0.8	V	
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA			−1.0	−1.5		−1.0	−1.5	V	1, 8
V_{OH}	High-Level Output Voltage (82S16)	V_{CC} = MIN, I_{OH} = −3.2mA		2.6			2.4			V	1, 6
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN, i_{OL} = 16mA			0.35	0.45		0.35	0.5	V	1, 7
I_{OLK}	Output Leakage Current (82S17)	V_{OUT} = 5.5V			1	40		1	40	μA	5
$I_{O(OFF)}$	Hi-Z State Output Current (82S16)	V_{OUT} = 5.5V			1	40		1	50	μA	5
		V_{OUT} = 0.45V			−1	−40		−1	−50	μA	5
I_{IH}	High-Level Input Current	V_{CC} = MAX, V_{IN} = 5.5V			1	25		1	25	μA	8
I_{IL}	Low-Level Input Current	V_{CC} = MAX, V_{IN} = 0.45V			−10	−100		−10	−250	μA	8
I_{OS}	Short-Circuit Output Current (82S16)	V_{CC} = MAX, V_O = 0V		−20		−70	−20		−70	mA	3
I_{CC}	V_{CC} Supply Current (82S16/17)	V_{CC} = MAX			80	115		80	120	mA	4
	V_{CC} Supply Current (82S16/17)	V_{CC} = MAX, T_A = +125°C							99	mA	4
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0V		5			5		pF	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V	V_{CC} = 5.0V		8			8		pF	

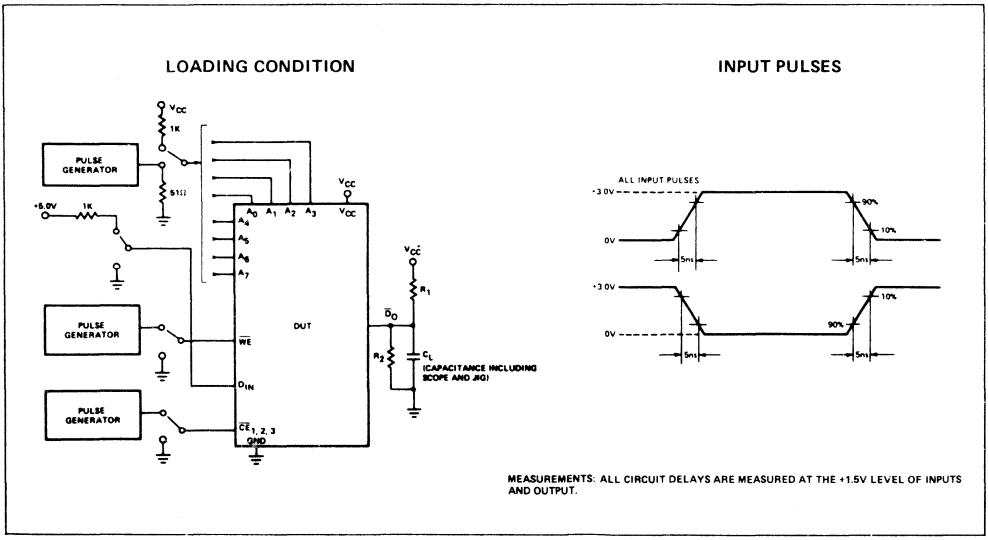
NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with a logic "0" stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to V_{CC}.
8. Test each input one at the time.

SWITCHING CHARACTERISTICS

S82S16/17 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S16/17 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S16/17			N82S16/17			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Propagation Delay									
T_{AA}	Address Access Time	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$		40	70		40	50	ns
T_{CE}	Chip Enable Access Time			30	40		30	40	ns
T_{CD}	Chip Enable Output Disable Time			30	40		30	40	ns
T_{WD}	Write Enable to Output Valid Time			30	55		30	40	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$	20	5		20	5		ns
T_{WSD}	Data In to Write Enable		50	40		40	30		ns
T_{WSC}	$\overline{CE}$ to Write Enable		10	0		10	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$	10	0		5	0		ns
T_{WHD}	Data In to Write Enable		10	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
T_{WP}	Write Enable Pulse Width	Note 2	40	20		30	15		ns

AC TEST LOAD

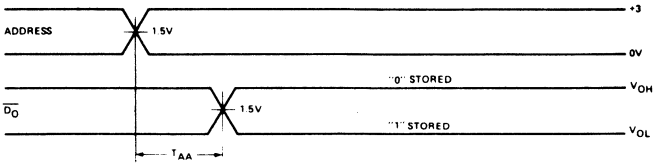


NOTES:
1. Typical values are at $V_{CC} = +5.0V$, and $T_A = +25°C$.
2. Minimum required to guarantee a WRITE into the slowest bit.

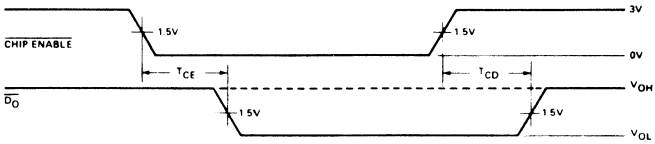
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

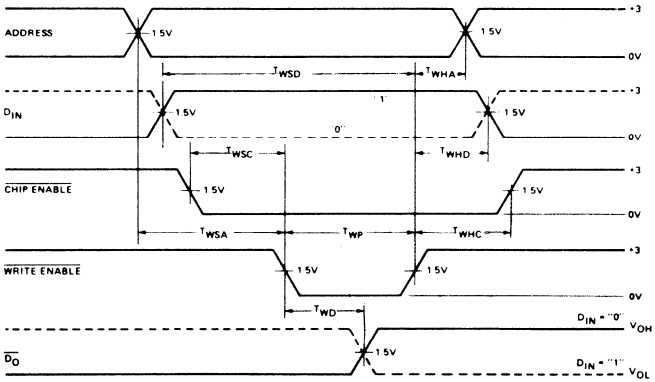
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.
T_{CD}	Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.
T_{AA}	Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.
T_{WSC}	Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.
T_{WHD}	Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.
T_{WP}	Width of WRITE ENABLE pulse.
T_{WSA}	Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.
T_{WSD}	Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.
T_{WD}	Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects complement of DATA INPUT.
T_{WHC}	Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.
T_{WHA}	Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

signetics

256-BIT BIPOLAR RAM (256x1 RAM) (82S116 TRI-STATE) (82S117 OPEN COLLECTOR)

82S116
82S117

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S116 and 82S117 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state output options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading to 25μA for a "1" level, and -100μA for a "0" level.

During WRITE operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both 82S116 and 82S117 devices are available in the commercial temperature range. For the commercial temperature range, (0°C to +75°C) specify N82S116/117, B or F.

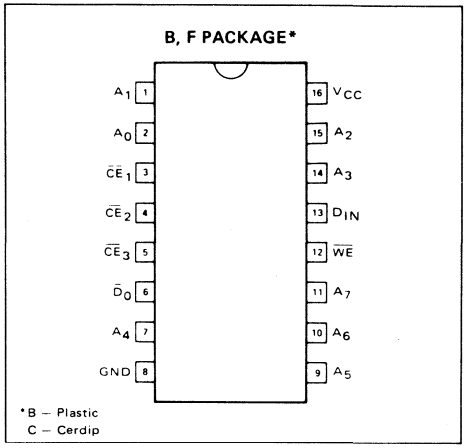
FEATURES

- ORGANIZATION – 256 X 1
- ADDRESS ACCESS TIME – 40ns, MAXIMUM
- WRITE CYCLE TIME – 25ns, MAXIMUM
- POWER DISSIPATION – 1.5mW/BIT TYPICAL
- INPUT LOADING – (-100μA) MAXIMUM
- OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
  TRI-STATE – 82S116
  OPEN COLLECTOR – 82S117
- 16 PIN CERAMIC DIP

APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION



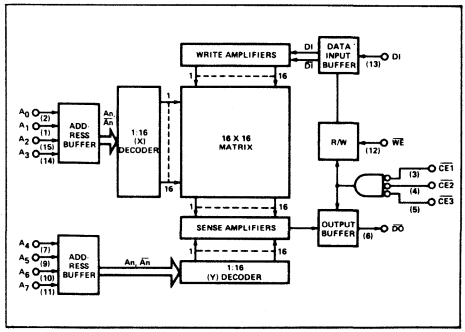
*B – Plastic
C – Cerdip

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82S116	82S117
READ	0	1	X	STORED $\overline{DATA}$	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1	1
WRITE "1"	0	0	1	0	0
DISABLED	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OUT}	High Level Output Voltage (82S117)	+5.5	Vdc
V_O	Off-State Output Voltage (82S116)	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

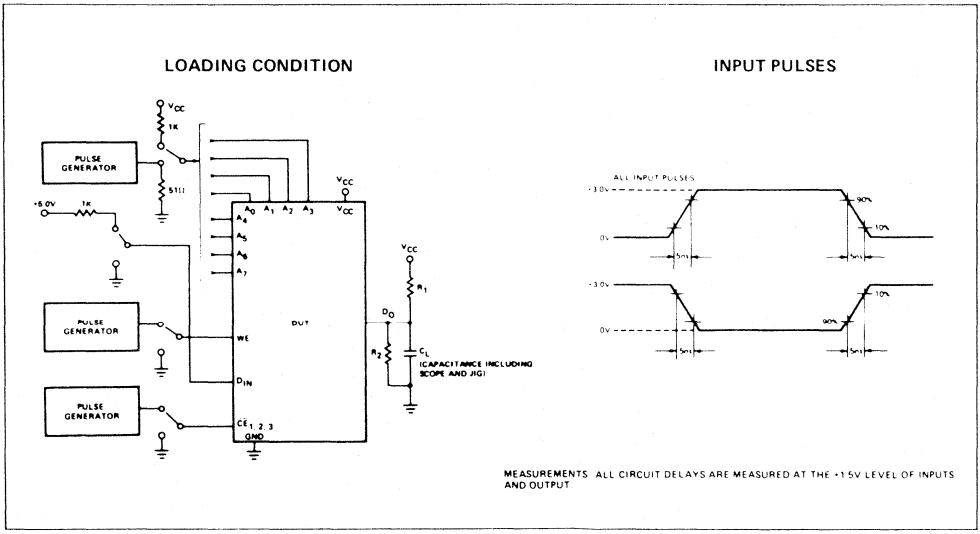
PARAMETER		TEST CONDITIONS		LIMITS			UNIT	NOTES
				MIN	TYP[2]	MAX		
V_{IH}	High-Level Input Voltage	V_{CC} = 5.25V		2.0			V	
V_{IL}	Low-Level Input Voltage	V_{CC} = 4.75V				0.85	V	1
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = −12 mA			−1.0	−1.5	V	1,8
V_{OH}	High-Level Output Voltage (82S116)	V_{CC} = 4.75V, I_{OH} = −3.2 mA		2.6			V	1,6
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.75V, I_{OL} = 16 mA			0.35	0.45	V	1,7
I_{OLK}	Output Leakage Current (82S117)	V_{OUT} = 5.5V			1	40	μA	5
$I_{O(OFF)}$	HI-Z State Output Current (82S116)	V_{OUT} = 5.5V			1	40	μA	5
		V_{OUT} = 0.45V			−1	−40	μA	5
I_{IH}	High-Level Input Current	V_{CC} = 5.25V, V_{IN} = 5.5V			1	25	μA	8
I_{IL}	Low-Level Input Current	V_{CC} = 5.25V, V_{IN} = 0.45V			−10	−100	μA	8
I_{OS}	Short-Circuit Output Current (82S116)	V_{CC} = 5.25V, V_O = 0V		−20		−70	mA	3
I_{CC}	V_{CC} Supply Current (82S116)	V_{CC} = 5.25V			80	115	mA	4
	V_{CC} Supply Current (82S117)	V_{CC} = 5.25V			80	115	mA	4
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0V		5		pF	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V			8		pF	

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Duration of the short circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with a logic "0" stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to V_{CC}.
8. Test each input one at the time.

SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C, 4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT	NOTE
			MIN	TYP[1]	MAX		
Propagation Delays							
T_{AA}	Address Access Time	$R_1 = 270\Omega$ $R_2 = 600\Omega$ $C_L = 30pF$		30	40	ns	
T_{CE}	Chip Enable Access Time			15	25	ns	
T_{CD}	Chip Enable Output Disable Time			15	25	ns	
T_{WD}	Write Enable to Output Disable Time			30	40	ns	
Write Set-up Times							
T_{WSA}	Address to Write Enable		0	-5		ns	
T_{WSD}	Data In to Write Enable		25	15		ns	
T_{WSC}	$\overline{CE}$ to Write Enable		0	-5		ns	
Write Hold Times							
T_{WHA}	Address to Write Enable		0	-5		ns	
T_{WHD}	Data In to Write Enable		0	-5		ns	
T_{WHC}	$\overline{CE}$ to Write Enable		0	-5		ns	
T_{WP}	Write Enable Pulse Width		25	15		ns	2

AC TEST LOAD

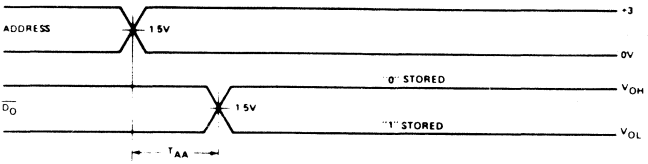


NOTES:
1. Typical values are at $V_{CC} = +5.0V$, and $T_A = +25°C$.
2. Minimum required to guarantee a WRITE into the slowest bit.

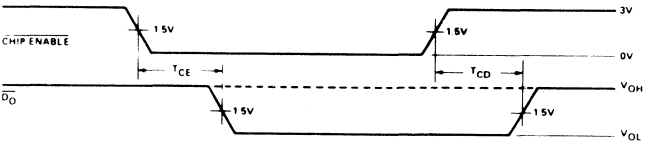
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

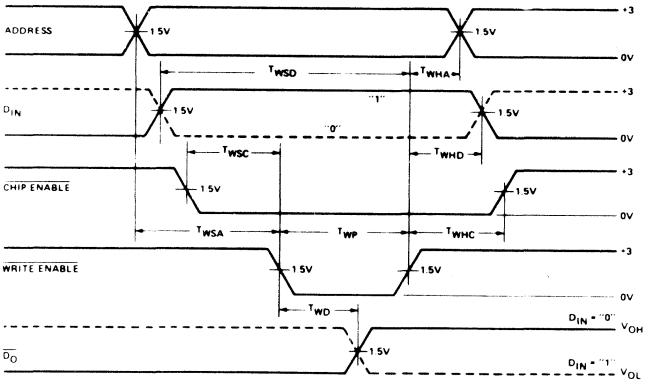
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects complement of DATA INPUT.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

signetics

TTL 256x1 RAM (54/74S200/201 TRI-STATE) (54/74S301 OPEN COLLECTOR)

54/74S200
54/74S201
54/74S301

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 54/74S200/201 and 54/74S301 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state outputs options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, three chip enable inputs and PNP input transistors which reduce input loading to 25μA for a "1" level and −250μA (S54S200/201/301) or −100μA (N74S200/201/301) for a "0" level.

The additional feature of output blanking during write ($\overline{D_O}$ terminal "H" or "Hi-Z" state) permits $\overline{D_O}$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. Both devices have fast read access and write cycle times and thus are ideally suited in high speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N74S200/201/301, B or F. For the military temperature range (−55°C to +125°C) specify S54S200/201/301, F only.

FEATURES

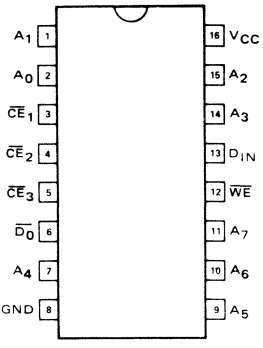
- ORGANIZATION – 256 X 1
- ADDRESS ACCESS TIME:
  S54S200/201/301 – 70ns MAXIMUM
  N74S200/201/301 – 50 ns MAXIMUM
- WRITE CYCLE TIME:
  S54S200/201/301 – 60ns MAXIMUM
  N74S200/201/301 – 50ns MAXIMUM
- POWER DISSIPATION – 1.5mW/BIT TYPICAL
- INPUT LOADING:
  S54S200/201/301 – (−250μA) MAXIMUM
  N74S200/201/301 – (−100μA) MAXIMUM
- OUTPUT BLANKING DURING WRITE
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
  TRI-STATE – 54/74S200/201
  OPEN COLLECTOR – 54/74S301
- 16 PIN CERAMIC DIP

APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

B, F PACKAGE*



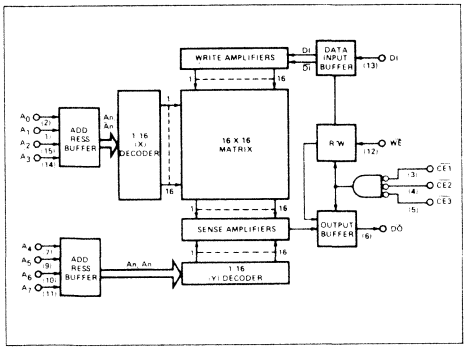
*B – Plastic
F – Cerdip

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				54/74S301	54/74S200/201
READ	0	1	X	STORED $\overline{DATA}$	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

*"0" = All $\overline{CE}$ inputs low; "1" = One or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OUT}	High Level Output Voltage (54/74S301)	+5.5	Vdc
V_O	Off-State Output Voltage (54/74S200/201)	+5.5	Vdc
T_A	Operating Temperature Range S54S200/201/301 N74S200/201/301)	 -55° to $+125^\circ$ 0° to $+70^\circ$	 °C °C
T_{stg}	Storage Temperature Range	-65° to $+150^\circ$	°C

ELECTRICAL CHARACTERISTICS

S54S200/201/301 $-55^\circ C \leq T_A \leq +125^\circ C$, $4.5V \leq V_{CC} \leq 5.5V$
N74S200/201/301 $0^\circ C \leq T_A \leq +70^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S54S200/201/301			N74S200/201/301			UNIT	NOTES
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX		
V_{IH}	High Level Input Voltage	V_{CC} = MAX	2.0			2.0			V	1
V_{IL}	Low Level Input Voltage	V_{CC} = MIN			0.8			0.85	V	1
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V	1, 8
V_{OH}	High Level Output Voltage (N74S200/201)	V_{CC} = MIN I_{OH} = −10.3mA				2.4			V	1, 6
V_{OH}	High Level Output Voltage (S54S200/201)	V_{CC} = MIN I_{OH} = −5.2mA	2.4						V	1, 6
V_{OL}	Low Level Output Voltage	V_{CC} = MIN I_{OL} = 16mA		0.35	0.50		0.35	0.45	V	1, 7
I_{OLK}	Output Leakage Current (54/74S301)	V_{CC} = MIN V_O = 2.4V		1	50		1	40	μA	5
		V_{IH} = 2V V_O = 5.5V		1	50		1	40	μA	5
$I_{O(OFF)}$	Hi-Z State Output Current (54/74S200/201)	V_{CC} = MAX V_O = 5.5V		1	50		1	40	μA	5
		V_{IH} = 2V V_O = 0.4V		−1	−50		−1	−40	μA	5
I_I	Input Current at V_{IN} MAX	V_{CC} = MAX, V_{IN} = 5.5V			1			1	mA	8
I_{IH}	High Level Input Current	V_{CC} = MAX, V_{IH} = 2.7V		1	25		1	25	μA	8
I_{IL}	Low Level Input Current	V_{CC} = MAX, V_{IL} = 0.45V		−10	−250		−10	−100	μA	8
I_{OS}	Short Circuit Output Current (54/74S200/201)	V_{CC} = MAX V_O = 0V	−30		−100	−30		−100	mA	3
I_{CC}	V_{CC} Supply Current (54/74S200/201/301)	V_{CC} = MAX		80	130		80	130	mA	4
	V_{CC} Supply Current (54S200/201/301)	V_{CC} = MAX, T_A = +125°C			99				mA	4
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5			5		pF	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V		8			8		pF	

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with logic "0" stored, and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to V_{CC}.
8. Test each input one at the time.

SWITCHING CHARACTERISTICS

S54S301 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N74S301 $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS		S54S301			N74S301			UNIT	NOTES[1]
		S54S301	N74S301	MIN	TYP[1]	MAX	MIN	TYP[1]	MAX		
t_{PLH} t_{PHL}	Access Time From Address				40 40	70 70		40 40	50 50	ns ns	B, D, E B, D, E
t_{PHL}	Enable Time From Chip Enable					45			35	ns	C, D, E
t_{PLH}	Disable Time From Chip Enable					30			20	ns	C, D, E
t_{PLH}	Disable Time From Write Enable					40			30	ns	C, D, E
t_{SR}	Sense-Recovery Time					50			40	ns	D
t_w	Width of Write Enable Pulse			50			40			ns	H
	Setup Time:										
	Address-to-Write Enable			0			0			ns	
t_{setup}	Data-to-Write Enable	$R_{L1} = 270\Omega$ $R_{L2} = 1K\Omega$	$R_{L1} = 270\Omega$ $R_{L2} = 1K\Omega$	50			40			ns	
	Chip Enable-to-Write Enable	$C_L = 15pF$	$C_L = 15pF$	0			0			ns	D
	Hold Time:										
	Address-From-Write Enable			10			10			ns	
t_{hold}	Data-From-Write Enable			10			10			ns	
	Chip Enable-From-Write Enable			0			0			ns	

SWITCHING CHARACTERISTICS

S54S200/201 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N74S200/201 $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$

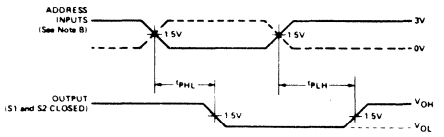
PARAMETER		TEST CONDITIONS		S54S200/201			N74S200/201			UNIT	NOTES[1]
		S54S200/201	N74S200/201	MIN	TYP[1]	MAX	MIN	TYP[1]	MAX		
t_{PLH} t_{PHL}	Access Time From Address	$R_L = 270\Omega$ $C_L = 15pF$	$R_L = 270\Omega$ $C_L = 15pF$		40 40	70 70		40 40	50 50	ns ns	B, D, E B, D, E
t_{ZH} t_{ZL}	Enable Time From Chip Enable					45 45			35 35	ns ns	C, D, F, G C, D, F, G
t_{HZ} t_{LZ}	Disable Time From Chip Enable	$R_L = 270\Omega$ $C_L = 5pF$	$R_L = 270\Omega$ $C_L = 5pF$			30 30			20 20	ns ns	C, D, F, G C, D, F, G
t_{HZ} t_{LZ}	Disable Time From Write Enable					40 40			30 30	ns ns	D, G D, G
t_{ZH} t_{ZL}	Sense-Recovery Time					50 50			40 40	ns ns	D, F D, F
t_w	Width of Write Enable Pulse			50			40			ns	H
	Setup Time:										
	Address-to-Write Enable			0			0			ns	
t_{setup}	Data-to-Write Enable	$R_L = 270\Omega$ $C_L = 15pF$	$R_L = 270\Omega$ $C_L = 15pF$	50			40			ns	
	Chip Enable-to-Write Enable			0			0			ns	D
	Hold Time:										
	Address-From-Write Enable			10			10			ns	
t_{hold}	Data-From-Write Enable			10			10			ns	
	Chip Enable-From-Write Enable			0			0			ns	

NOTES: 1. All typical values are $V_{CC} = 5V$, $T_A = 25°C$. 2. See Notes on Switching Parameter Measurement Information.

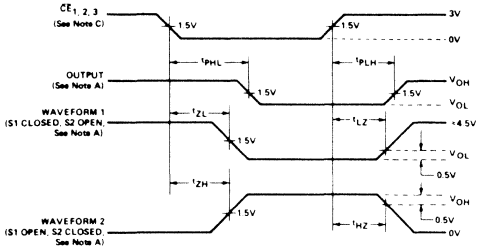
SWITCHING PARAMETER MEASUREMENT INFORMATION

READ CYCLE

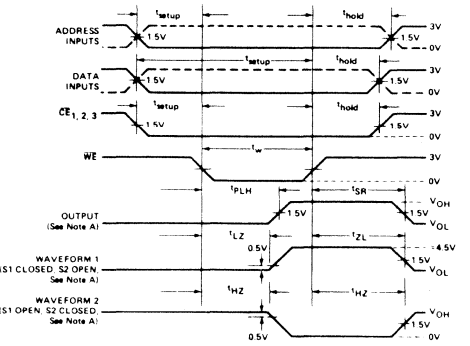
ACCESS TIME FROM ADDRESS



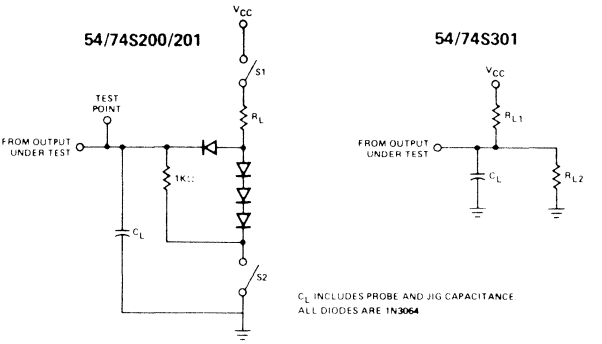
CHIP ENABLE AND DISABLE TIME



WRITE CYCLE



AC TEST LOAD



NOTES:

A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.

C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.

D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ns, $t_f \leq 2.5$ns, PRR ≤ 1MHz, and $Z_{out} \approx 50\Omega$.

E. t_{PLH} propagation delay time, low-to-high level output, t_{PHL} propagation delay time, high-to-low-level output.

F. t_{ZH} propagation delay time, hi-Z to high-level output, t_{ZL} propagation delay time, hi-Z to low-level output.

G. t_{HZ} propagation delay time, high-level to hi-Z output, t_{LZ} propagation delay time, low-level to hi-Z output.

H. Minimum required to guarantee a WRITE into the slowest bit.

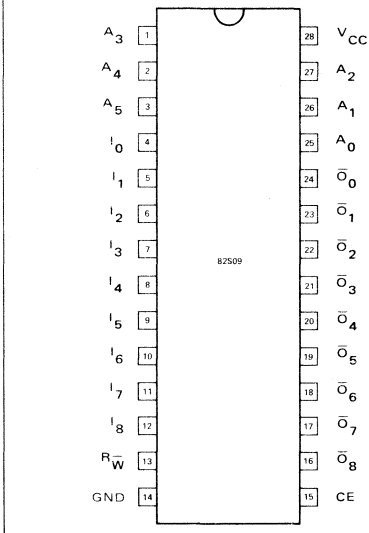
PRELIMINARY SPECIFICATIONS **DIGITAL 8000 SERIES TTL/MEMORY**

DESCRIPTION

The 82S09 is a 576 bit, TTL compatible, random access memory organized as 64 words by 9 bits per word. It is ideally suited for scratch pad, small buffer, and other applications where the number of words is limited and the number of bits per word is relatively large. The ninth bit provides a parity bit for 8 bits/word systems.

PIN CONFIGURATION

I PACKAGE



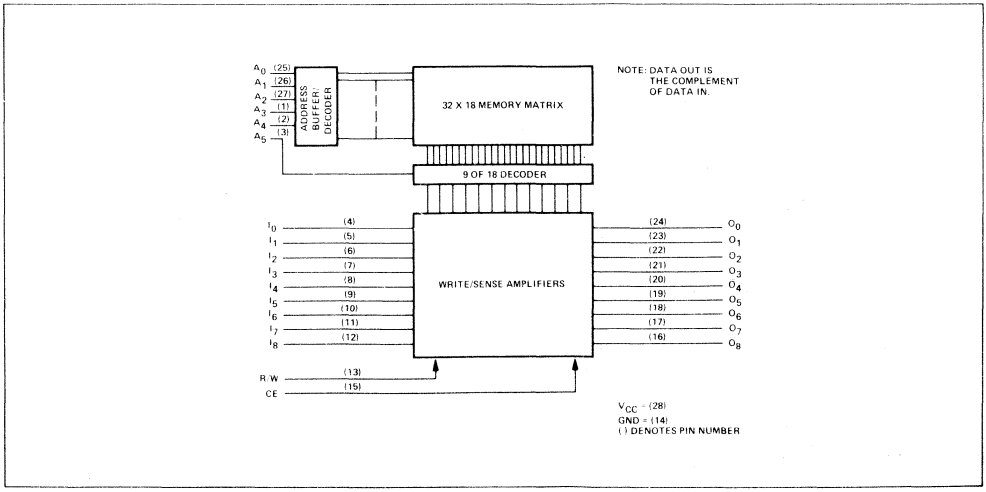
FEATURES

- 64 X 9 ORGANIZATION
- 30 nSEC TYPICAL ACCESS TIME
- 1.5 mW/BIT TYPICAL POWER DISSIPATION
- 100μA INPUT LOAD
- OPEN-COLLECTOR OUTPUT

APPLICATIONS

SCRATCH PAD
BUFFER MEMORIES
CONTROL STORE

BLOCK DIAGRAM



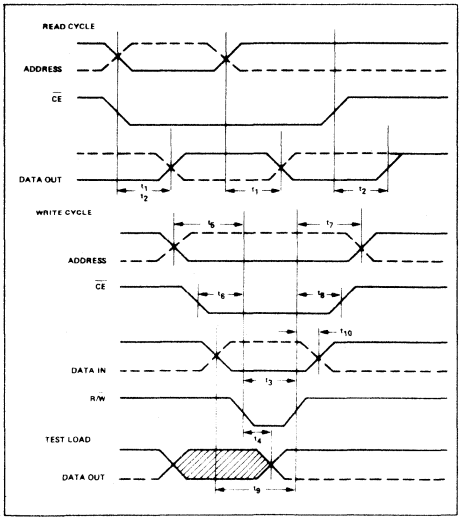
OBJECTIVE ELECTRICAL CHARACTERISTICS $0 \geq T_A \geq 75°C, 4.75 \geq V_{CC} \geq 5.25V$

CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITION
"O" Input Current			-100	μA	V_{IN} = 0.45V
"I" Input Current			25	μA	V_{IN} = 5.25V
Input Clamp Voltage			-1.2	Volts	I_{IN} = 18mA
"O" Input (V_{IL})			0.85	Volts	
"I" Input (V_{IH})	2.0			Volts	
Output Leakage			40	μA	V_{OUT} = 5.5V
"O" Output Voltage			0.5	Volts	I_{OUT} = -6.4mA
Power Supply Current		170	200	mA	

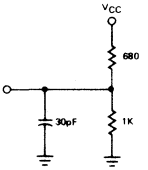
OBJECTIVE SWITCHING CHARACTERISTICS $0 \geq T_A \geq 75°C, 4.75 \geq V_{CC} \geq 5.25V$

CHARACTERISTIC		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITION
Access Time						
Address to Output	t_1		35	50	nS	
$\overline{CE}$ to Output	t_2		35	50	nS	
Write Pulse Width	t_3	45			nS	
Write Access Time	t_4		35	50	nS	Data Stable Prior to Write
Address/$\overline{CE}$ Set-Up	t_5/t_6	10			nS	
Address/$\overline{CE}$ Hold	t_7/t_8	10			nS	
Data Set-Up	t_9	50			nS	
Data Hold	t_{10}	5			nS	

TIMING DIAGRAM



TEST LOAD



signetics

1024x1 BIT BIPOLAR RAM OPEN COLLECTOR (82S10) TRI-STATE (8211)

82S10 82S11

FEBURARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

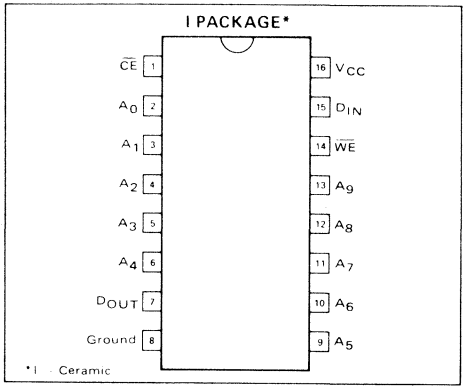
DESCRIPTION

The 82S10/11 is a high speed 1024-bit random access memory organized as 1024 words X 1 bit. With a typical access time of 30ns, it is ideal for cache buffer applications and for systems requiring very high speed main memory.

Both the 82S10 and 82S11 require a single +5 volts power supply and feature very low current PNP input structures. They are fully TTL compatible, and include on-chip decoding and a chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S10 and 82S11 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S10/11, I. For the military temperature range (−55°C to +125°C) specify S82S10/11, I.

PIN CONFIGURATION



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				82S10	82S11
READ	0	1	X	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

X = Don't care.

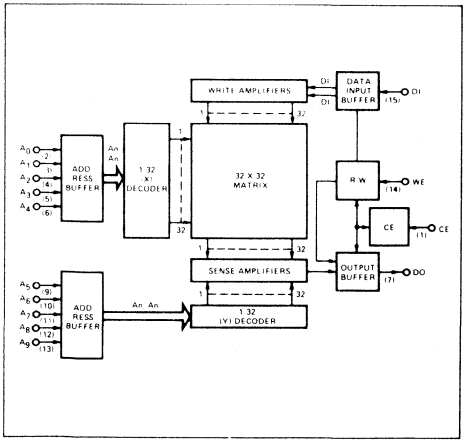
FEATURES

- ORGANIZATION – 1024 X 1
- ADDRESS ACCESS TIME:
  S82S10/11 – 70ns, MAXIMUM
  N82S10/11 – 45ns, MAXIMUM
- WRITE CYCLE TIME:
  S82S10/11 – 75ns, MAXIMUM
  N82S10/11 – 45ns, MAXIMUM
- POWER DISSIPATION – 0.5mW/BIT, TYPICAL
- INPUT LOADING:
  S82S10/11 – (−150μA) MAXIMUM
  N82S10/11 – (−100μA) MAXIMUM
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
  82S10 – OPEN COLLECTOR
  82S11 – TRI-STATE
- NON-INVERTING OUTPUT
- BLANKED OUTPUT DURING WRITE
- 16 PIN CERAMIC PACKAGE

APPLICATIONS

HIGH SPEED MAIN FRAME
CACHE MEMORY
BUFFER STORAGE
WRITABLE CONTROL STORE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S10)	+5.5	Vdc
V_O	Off-State Output Voltage (82S11)	+5.5	Vdc
T_A	Operating Temperature Range (N82S10/11) (S82S10/11)	 0° to +75° −55° to +125°	 °C °C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS[9]

S82S10/11 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S10/11 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	S82S10/11			N82S10/11			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage	V_{CC} = MIN (Note 1)			.80			.85	V
V_{IH}	High Level Input Voltage	V_{CC} = MAX (Note 1)	2.1			2.1			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA (Note 1, 7)		−1.0	−1.5		−1.0	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = MIN, I_{OL} = 16mA (Note 1, 8)		0.35	0.50		0.35	0.45	V
V_{OH}	High Level Output Voltage (82S11)	V_{CC} = MIN, I_{OH} = −2mA (Note 1, 5)	2.4			2.4			V
I_{OLK}	Output Leakage Current (82S10)	V_{CC} = MAX, V_{OUT} = 5.5V (Note 6)		1	60		1	40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S11)	V_{CC} = MAX, V_{OUT} = 5.5V V_{CC} = MAX, V_{OUT} = 0.45V (Note 6)		1 −1	100 −100		1 −1	60 −60	μA μA
I_{IL}	Low Level Input Current	V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	High Level Input Current	V_{IN} = 5.5V		1	40		1	25	μA
I_{OS}	Short Circuit Output Current (82S11)	V_{CC} = MAX, V_{OUT} = 0V (Note 3)	−20		−100	−20		−100	mA
I_{CC}	V_{CC} Supply Current	V_{CC} = MAX (Note 4) $0 < T_A < 25°C$ $T_A \geq 25°C$ $T_A \leq 0°C$		 120 95	 155 130 170		 120 95	 155 130 170	 mA mA mA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		4			4		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V		7			7		pF

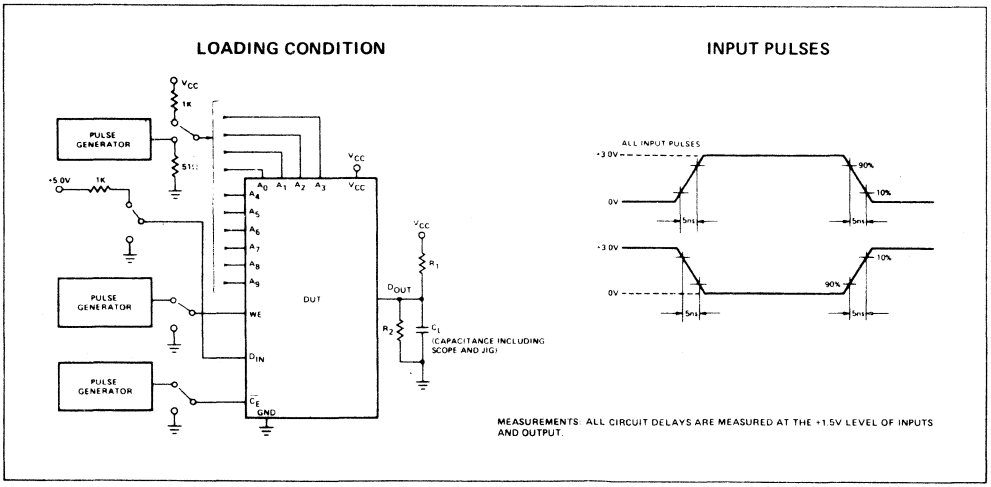
NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of the short circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic "1" stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Test each input one at the time.
8. Measured with a logic "0" stored. Output sink current is supplied through a resistor to V_{CC}.
9. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm up. Typical thermal resistance values of the package at maximum temperature are:
   ϕ_{JA} Junction to Ambient at 400 lpm air flow = 50°C/Watt
   ϕ_{JA} Junction to Ambient = still air = 90°C/Watt
   ϕ_{JA} Junction to Case = 20°C/Watt

SWITCHING CHARACTERISTICS[3]

S82S10/11 $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, $4.5V \leq V_{CC} \leq 5.5$
N82S10/11 $0^{\circ}C \leq T_A \leq +75^{\circ}C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	S82S10/11			N82S10/11			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Propagation Delays									
T_{AA}	Address Access Time	C_L = 30pF R_1 = 270Ω R_2 = 600Ω		30	70		30	45	ns
T_{CE}	Chip Enable Access Time			15	45		15	30	ns
T_{CD}	Chip Enable Output Disable Time			15	45		15	30	ns
T_{WD}	Write Enable to Output Disable Time			20	45		20	30	ns
T_{WR}	Write Recovery Time			20	45		20	30	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable		15	0		5	0		ns
T_{WSD}	Data In to Write Enable		55	35		40	35		ns
T_{WSC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		5	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 2)		50	25		35	25		ns

AC TEST LOAD

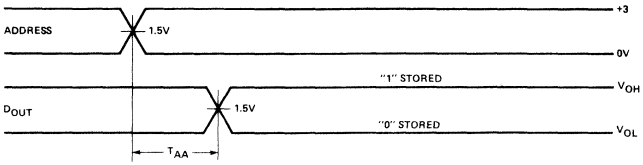


NOTES:
1. Typical values are at V_{CC} = +5.0V, and T_A = +25°C.
2. Minimum required to guarantee a WRITE into the slowest bit.
3. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} Junction to Ambient at 400 fpm air flow – 50°C/Watt
   θ_{JA} Junction to Ambient – still air – 90°C/Watt
   θ_{JA} Junction to Case – 20°C/Watt

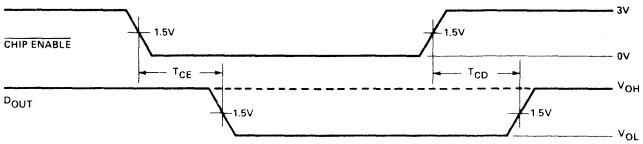
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

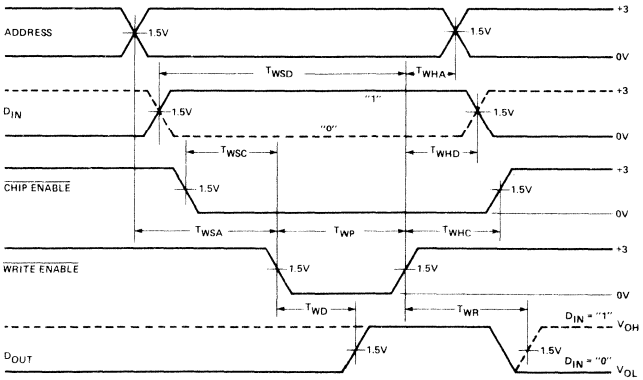
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid—not as shown.)

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid. .

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

signetics

256×1 STATIC READ/WRITE RANDOM ACCESS MEMORY

2501

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2500 Series 256 x 1 Random Access Memory employs enhancement mode P-channel MOS devices integrated on a single monolithic chip. It is fully decoded, permitting the use of a 16-pin dual in-line package. Complete static operation requires no clocking.

FEATURES

- FULLY DECODED ADDRESSES
- ACCESS TIME – 1.0μs GUARANTEED
- POWER DISSIPATION: 1.6mW/BIT MAXIMUM
- STANDBY POWER DISSIPATION: 150μW/BIT
- DTL AND TTL COMPATIBLE
- CHIP SELECT AND OUTPUT WIRED-OR CAPABILITY
- STANDARD 16-PIN DIP
- P-MOS SILICON GATE TECHNOLOGY
- V_{CC} = +5V, V_{DD} = V_D = -9V

APPLICATIONS

SMALL BUFFER STORES
SMALL CORE MEMORY REPLACEMENT
BIPOLAR COMPATIBLE DATA STORAGE

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PROCESS TECHNOLOGY

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

BIPOLAR COMPATIBILITY

All inputs of the 2501 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6 mA, sufficient to drive one standard TTL load.

POWER DISSIPATION

The maximum power dissipation of 1.6mW/bit is required only during Read or Write. For standby operation, 150μW/bit is obtained by removing V_D and reducing V_{DD} to -4.0V. Removal of V_D alone will cut power dissipation by a factor of 1.5.

SPECIAL FEATURE

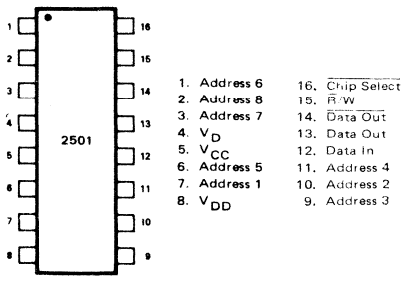
The outputs of the 2501 are effectively open circuited when the device is not selected (logic 1 on chip select). This feature allows OR-Tying for memory expansion.

PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP. RANGE
2501B	16-pin Silicone DIP	0°C. to +70°C.
2501I	16-pin Ceramic DIP	0°C. to +70 C.

PIN CONFIGURATION (Top View)

B/I PACKAGE



MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.3V to -20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	-18V
Power Dissipation at T_A = 70°C	640mW

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

NOTE: Special devices are available for operation at V_{DD} = -7V, V_D = -10V. Contact your Signetics Representative for details.

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V (8), V_{DD} = V_D = -9V ±5%, unless otherwise specified. See notes below)

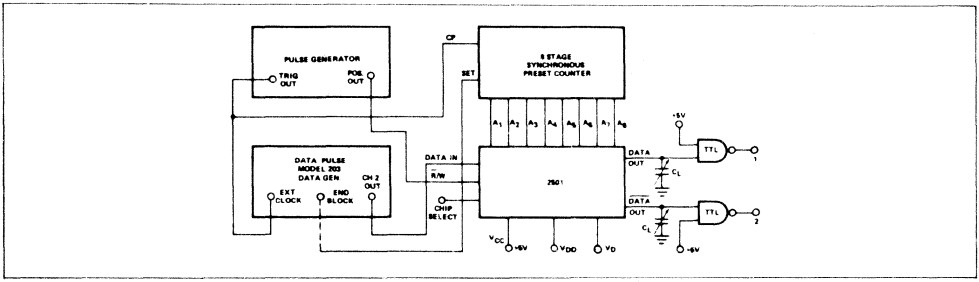
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)		<1.0	500	nA	V_{IN} = 0.0V; T_A = +25°C
I_{LO}	Output Leakage Current		<1.0	1000	nA	V_{OUT} = 0.0V, Chip Select Input = +3.3V, T_A = +25°C
I_{DD}	Power Supply Current, V_{DD}		13.0	18	mA	T_A = +25°C, V_{DD} = V_D = −9V
I_D	Power Supply Current, V_D		8.5	12	mA	I_{OL} = 0.0mA T_A = +25°C V_{DD} = V_D = −9V
V_{IL}	Input "Low" Voltage	−12		V_{CC}−4.5	V	
V_{IH}	Input "High" Voltage	V_{CC}−2.0		V_{CC}+0.3	V	
I_{OL1}	Output Sink Current	3.0	6		mA	V_{OUT} = +0.45V, T_A = +25°C
I_{OL2}	Output Sink Current	2.0	5		mA	V_{OUT} = +0.45V, T_A = +70°C
I_{OL3}	Output Sink Current		6	13	mA	V_{OUT} = −0.7 V
I_{OH1}	Output Source Current	−3.0	4		mA	V_{OUT} = 0.0V, T_A = +25°C
I_{OH2}	Output Source Current	−2.0	3		mA	V_{OUT} = 0.0V, T_A = +70°C
V_{OL}	Output "Low" Voltage		−0.7	+0.45	V	I_{OL} = 3.0 mA
V_{OH}	Output "High" Voltage	+3.5	+4.5		V	I_{OH} = −100μA
C_{IN}	Input Capacitance (All Input Pins)		7	10	pF	V_{IN} = +5.0V f = 1 MHz
C_{OUT}	Output Capacitance		7	10	pF	V_{OUT} = +5.0 V f = 1 MHz

SWITCHING CHARACTERISTICS

Guaranteed Limits $T_A = 0^\circ$ C to $+70^\circ$C, $V_{CC} = +5V$ (8) , $V_{DD} = V_D = -9V \pm 5\%$ except as noted.

READ CYCLE			WRITE CYCLE		
SYMBOL	TEST	LIMITS (μsec) MAX	SYMBOL	TEST	LIMITS (μsec) MIN.
t_a	Access Time	1.0μsec	t_{WD}	Address to Write Pulse Delay	0.3
			t_{WP}	Write Pulse Width	0.4
			t_W	Write Time	0.3
			t_{DO}	Data-Write Pulse Overlap	0.1

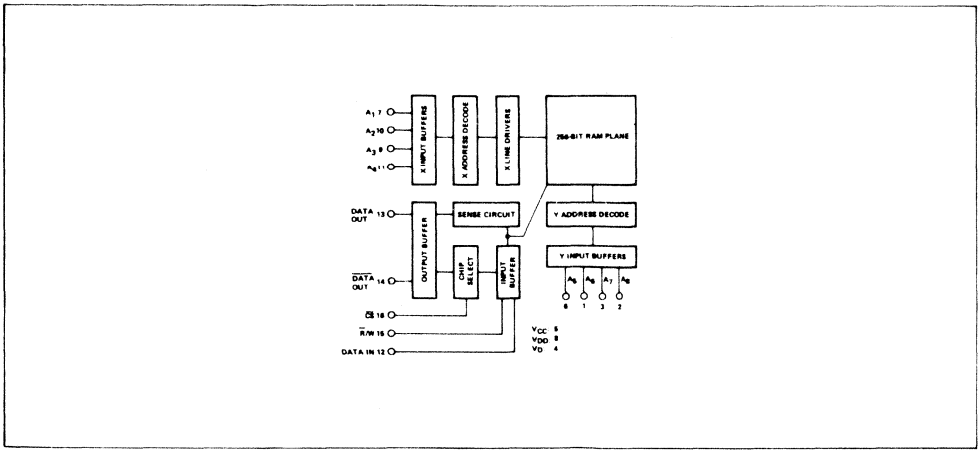
TEST SETUP FOR SPEED MEASUREMENT



NOTES:

1. Each clock time is split into a Read followed by a Write. Read and Write times can be varied by adjustment of the "delay" and "width" controls of the pulse generator.
2. Data generator produces a 256-bit block of data, 32 bits repeated 8 times. "PCM" mode used so data can be changed in 32 bits of the 2501 from one cycle to the next.
3. All inputs to the 2501 are standard TTL outputs with $V_{CC} = +5V \pm 5\%$.
4. Access time is measured between A1 (least significant address input) and points 1 and 2.

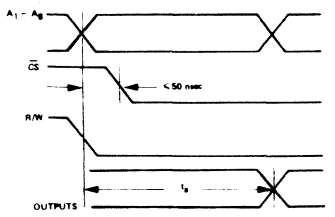
BLOCK DIAGRAM



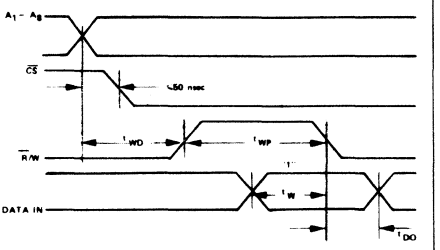
CONDITIONS OF TEST

Input pulse amplitudes: 0 to +5V, Input pulse rise and fall times: < 10 nsec. Speed measurements referenced to 1.5V levels. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{pd} \leq 10$ nsec)

READ CYCLE (For Measurement Purpose Only)

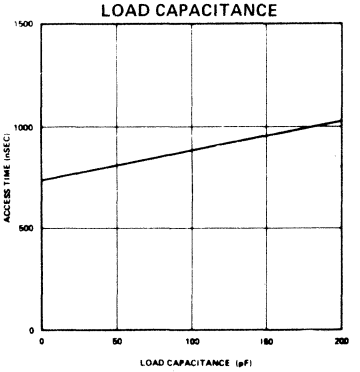


WRITE CYCLE (For Measurement Purpose Only)

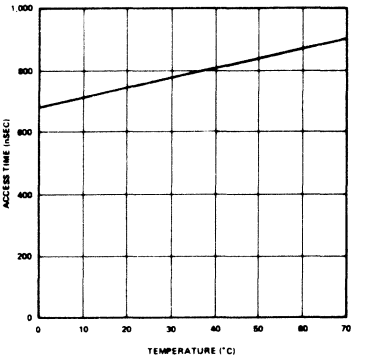


TYPICAL CHARACTERISTICS

ACCESS TIME VERSUS LOAD CAPACITANCE



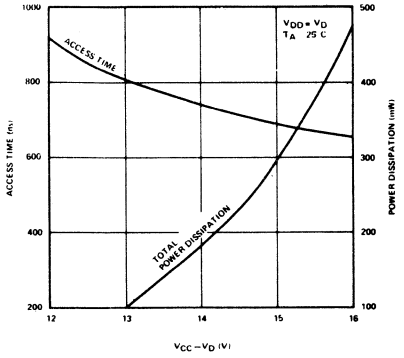
ACCESS TIME VERSUS TEMPERATURE



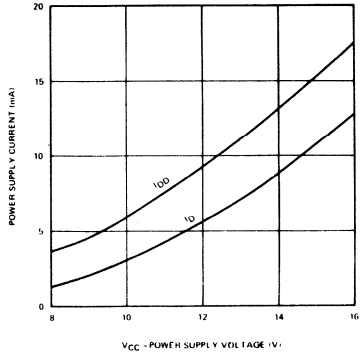
NOTE:
For all typical curves, $V_{CC} = 5V$, $V_{DD} = V_D = -9V$, $T_A = 25^{\circ}C$ (unless otherwise noted).

TYPICAL CHARACTERISTICS (Cont'd)

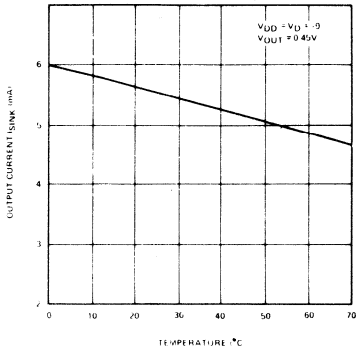
TYPICAL ACCESS TIME AND POWER DISSIPATION VERSUS SINGLE POWER SUPPLY VOLTAGE



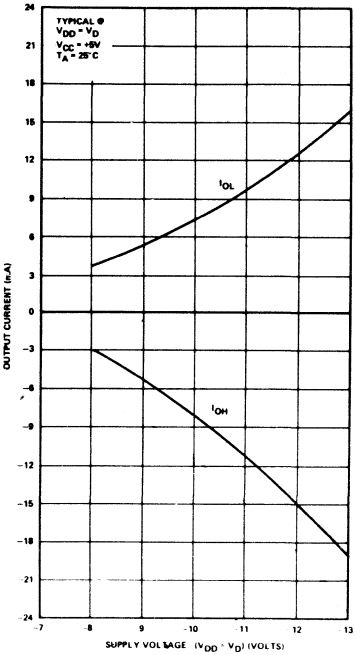
POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



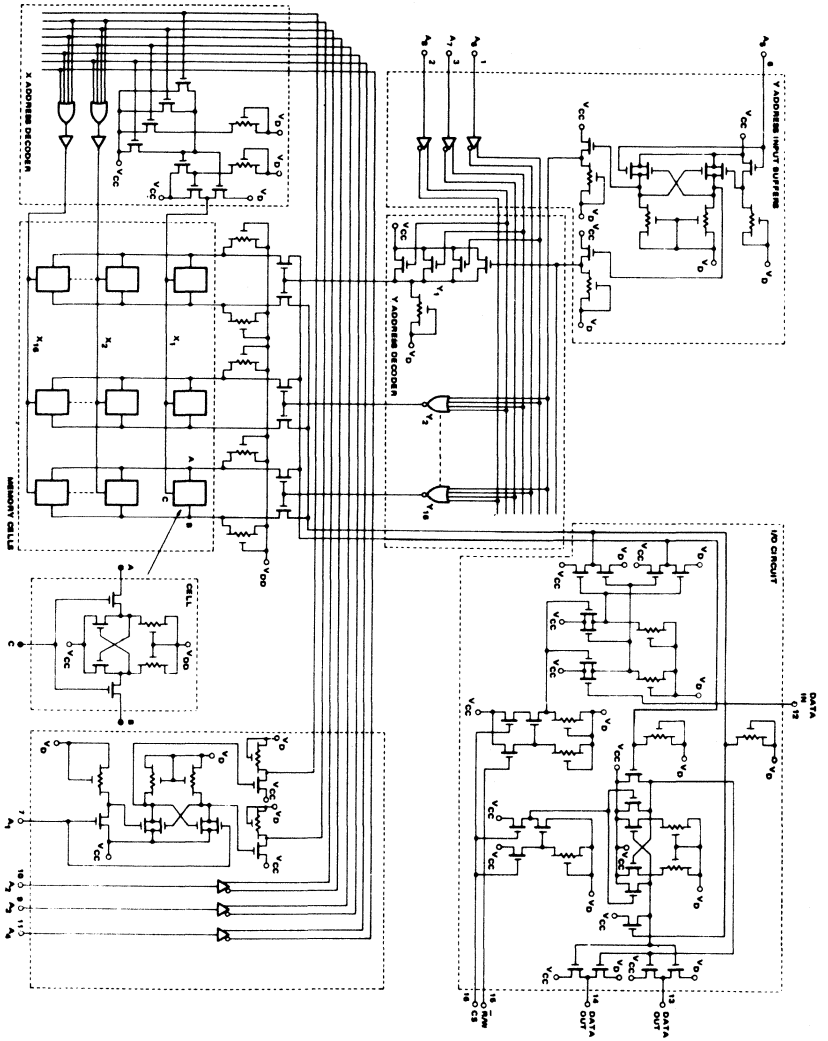
OUTPUT CURRENT VERSUS TEMPERATURE



OUTPUT CURRENT VERSUS SUPPLY VOLTAGE



CIRCUIT SCHEMATIC



Signetics 2501 256 X 1 Static Random Access Memory

signetics

256×1 STATIC READ/WRITE RANDOM ACCESS MEMORY | 25L01

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 25L01-256 x 1 Random Access Memory employs enhancement mode P-channel MOS devices integrated on a single monolithic chip. It is fully decoded, permitting the use of a 16-pin dual in-line package. Complete static operation requires no clocking. The 25L01 is optimized with +5 and -12V supplies.

FEATURES

- **FULLY DECODED ADDRESSES**
- **ACCESS TIME: 1.0 μs GUARANTEED**
- **POWER DISSIPATION: 1.7 MW/BIT MAXIMUM**
- **STANDBY POWER DISSIPATION: 100 μW/BIT**
- **DTL AND TTL COMPATIBLE**
- **CHIP SELECT AND OUTPUT WIRED-OR CAPABILITY**
- **STANDARD 16-PIN DIP**
- **P-MOS SILICON GATE TECHNOLOGY**
- **V_{CC} = +5V, V_{DD} = V_D = -12V**

APPLICATIONS

SMALL BUFFER STORES
SMALL CORE MEMORY REPLACEMENT
BIPOLAR COMPATIBLE DATA STORAGE

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

BIPOLAR COMPATIBILITY

All inputs of the 25L01 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6 mA, sufficient to drive one standard TTL load.

POWER DISSIPATION

The maximum power dissipation of 1.7 mW/bit is required only during Read or Write. For standby operation 100 μW/bit is obtained by removing V_D and reducing V_{DD} to −8.0V. Removal of V_D alone will cut power dissipation by a factor of almost 3.

TRI-STATE OUTPUT

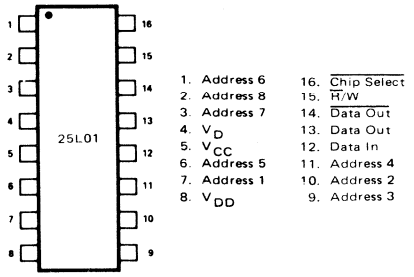
The outputs of the 25L01 are effectively open circuited when the device is not selected (logic 1 on chip select). This feature allows OR-tieing for memory expansion.

PART IDENTIFICATION TABLE

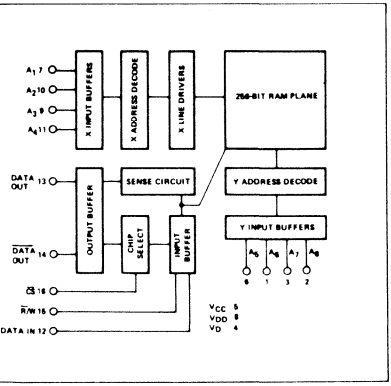
TYPE	PACKAGE	OP. TEMP. RANGE
25L01B	16-pin Silicone DIP	0°C to +70°C
25L01I	16-pin Ceramic DIP	0°C to +70°C

PIN CONFIGURATION (Top View)

B/I PACKAGE



BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.3V to -20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	-18V
Power Dissipation at T_A = 25°C "B" pkg.	640 mW
"I" pkg.	800 mW

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient ("B" pkg.) ("I" pkg., 100°C/W).
3. All inputs protected against static charge.
4. Parameter valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.

DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{DD} = V_D = -12V ± 5% unless otherwise specified. See notes above).

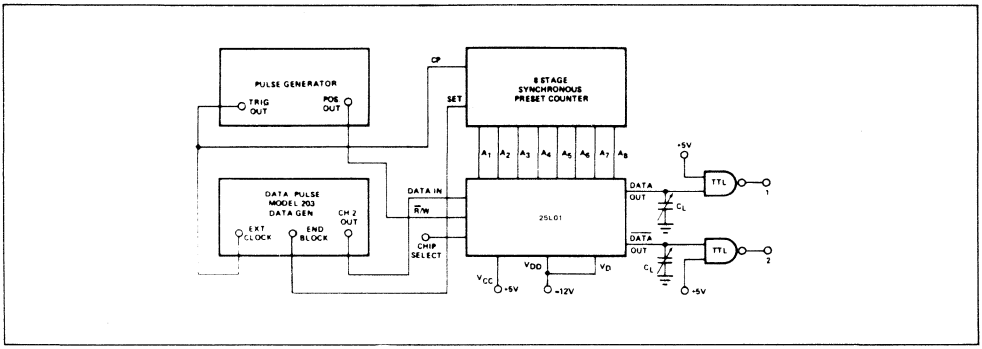
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)		<1.0	500	nA	V_{IN} = 0.0V; T_A = +25°C
I_{LO}	Output Leakage Current		<1.0	1000	nA	V_{OUT} = 0.0V, Chip Select Input = +3.3V, T_A = +25°C
I_{DD}	Power Supply Current, V_{DD}		5	9	mA	T_A = +25°C
I_D	Power Supply Current, V_D		11	16	mA	I_{OL} = 0.0 mA T_A = +25°C
V_{IL}	Input "Low" Voltage	-12		V_{CC}-4.5	V	
V_{IH}	Input "High" Voltage	V_{CC}-2.0		V_{CC}+0.3	V	
I_{OL1}	Output Sink Current	3.0	6		mA	V_{OUT} = +0.45V, T_A = +25°C
I_{OL2}	Output Sink Current	2.0	5		mA	V_{OUT} = +0.45V, T_A = +70°C
I_{OL3}	Output Sink Current		6	13	mA	V_{OUT} = -0.7 V
I_{OH1}	Output Source Current	-3.0	4		mA	V_{OUT} = 0.0V, T_A = +25°C
I_{OH2}	Output Source Current	-2.0	3		mA	V_{OUT} = 0.0V, T_A = +70°C
V_{OL}	Output "Low" Voltage		-0.7	+0.45	V	I_{OL} = 3.0 mA
V_{OH}	Output "High" Voltage	+3.5	+4.5		V	I_{OH} = -100μA
C_{IN}	Input Capacitance (All Input Pins)		7	10	pF	V_{IN} = +5.0V f = 1 MHz
C_{OUT}	Output Capacitance		7	10	pF	V_{OUT} = +5.0 V f = 1 MHz

SWITCHING CHARACTERISTICS

Guaranteed Limits T_A = 0 to +70°C, V_{CC} = +5V ±5%, V_{DD} = V_D = -12V ±5%

READ CYCLE			WRITE CYCLE		
SYMBOL	TEST	LIMITS (μsec) MAX	SYMBOL	TEST	LIMITS (μsec) MIN.
t_a	Access Time	1 μsec	t_{WD}	Address to Write Pulse Delay	0.3
			t_{WP}	Write Pulse Width	0.4
			t_W	Write Time	0.3
			t_{DO}	Data-Write Pulse Overlap	0.1

TEST SETUP FOR SPEED MEASUREMENT



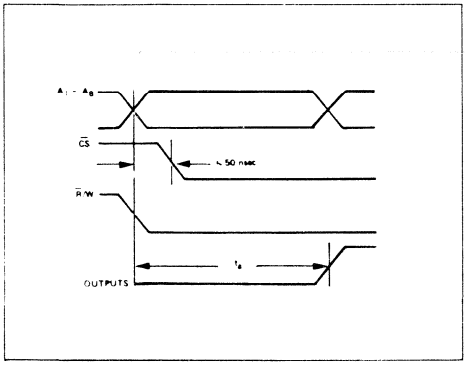
NOTES:

1. Each clock time is split into a Read followed by a Write. Read and Write times can be varied by adjustment of the "delay" and "width" controls of the pulse generator.
2. Data generator produces a 256-bit block of data, 32 bits repeated 8 times. "PCM" mode used so data can be changed in 32 bits of the 25L01 from one cycle to the next.
3. All inputs to the 25L01 are standard TTL outputs with V_{CC} = +5V ±5%.
4. Access time is measured between A1 (least significant address input) and points 1 and 2.

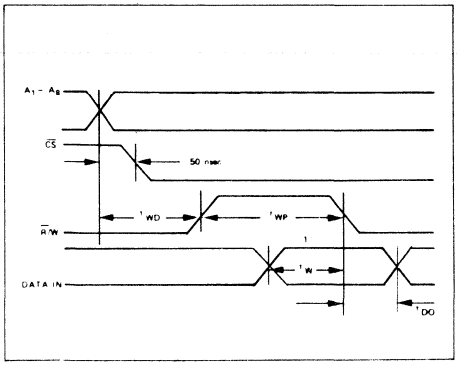
CONDITIONS OF TEST

Input pulse amplitudes: 0 to +5V, Input pulse rise and fall times: < 10 nsec. Speed measurements referenced to 1.5V levels. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{pd} \leq$ 10 nsec).

READ CYCLE (For Measurement Purpose Only)



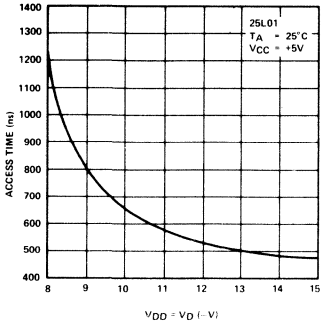
WRITE CYCLE (For Measurement Purpose Only)



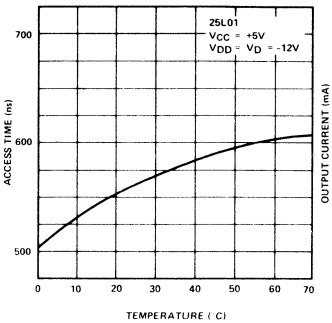
APPLICATION INFORMATION: Reference 2501 specifications.

TYPICAL CHARACTERISTIC CURVES

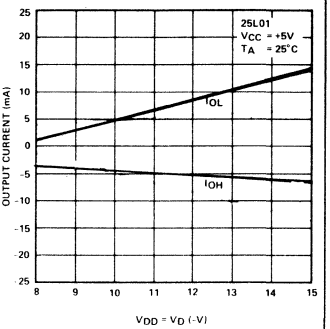
ACCESS TIME VERSUS SUPPLY VOLTAGE



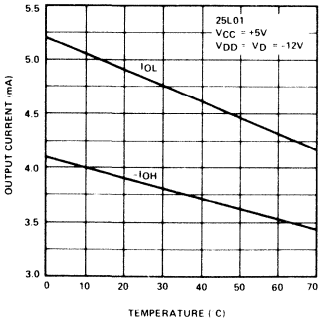
ACCESS TIME VERSUS TEMPERATURE



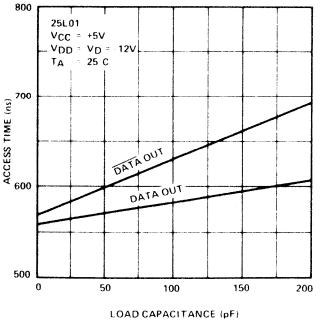
OUTPUT CURRENT VERSUS SUPPLY VOLTAGE



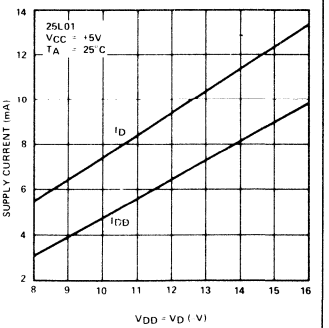
OUTPUT CURRENT VERSUS TEMPERATURE



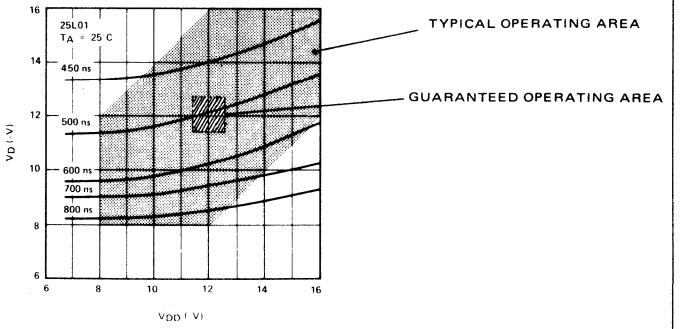
ACCESS TIME VERSUS LOAD CAPACITANCE



POWER SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



ACCESS TIME VERSUS SUPPLY VOLTAGES



DESCRIPTION

The Signetics 1103 is designed for main memory applications where high performance, low cost and large bit storage are important design objectives. It is a 1024 word by 1 bit random access memory element using enhancement mode P-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18-pin dual in-line package. The dynamic circuitry dissipates significant power only during precharge. Information stored in the memory is nondestructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds. A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied. Use Signetics 8T25 Sense Amp, and 3207 Clock Driver.

FEATURES

- **LOW POWER DISSIPATION – DISSIPATES POWER PRIMARILY ON SELECTED CHIPS**
- **ACCESS TIME – 300 nsec.**
- **CYCLE TIME – 580 nsec.**
- **REFRESH PERIOD – 2 MILLISECONDS FOR 0-70°C AMBIENT**
- **OR-TIE CAPABILITY**
- **SIMPLE MEMORY EXPANSION WITH CHIP ENABLE**
- **FULLY DECODED – ON-CHIP ADDRESS DECODE**
- **INPUTS PROTECTED – ALL INPUTS HAVE PROTECTION AGAINST STATIC CHARGE.**
- **LOW COST PACKAGING –18 PIN SILICONE AND 18 PIN CERAMIC DUAL IN-LINE**

APPLICATIONS

CORE MEMORY REPLACEMENT
BUFFER STORES
MAIN MEMORY

PROCESS TECHNOLOGY

The use of Signetics' unique silicon gate low threshold process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

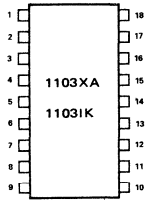
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric

SILICONE PACKAGING (Cont'd)

material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PIN CONFIGURATION (Top View)

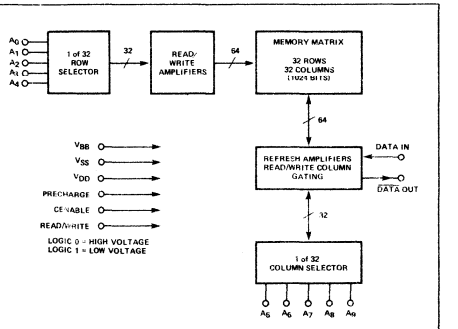


1. Address 3
2. Address 2
3. Address 0
4. Address 1
5. Precharge
6. Address 9
7. Address 6
8. Address 5
9. Address 7
18. Read/write
17. V_{SS}
16. Cenable
15. Address 4
14. $\overline{\text{Data}}$ Out
13. Address 8
12. Data In
11. V_{DD}
10. V_{BB}

PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP. RANGE
1103XA	18-Pin DIP Silicone	0-70°C
1103IK	18-Pin DIP Ceramic	0-70°C

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS(10)

Operating Ambient Temperature	0°C to 70°C	Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to +0.8V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.0W
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{BB}	−25V to +0.8V		

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS}(1) = 16V ± 5%, (V_{BB} − V_{SS})(6) = 3V to 4V, V_{DD} = 0V unless otherwise specified (Note 9).

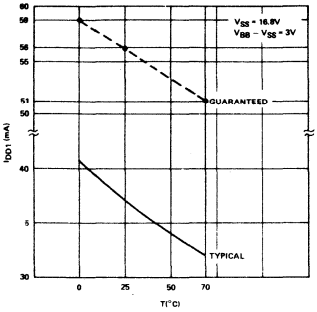
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All input pins)			1	μA	V_{IN} = 0V, T_A = 25°C
I_{LO}	Output Leakage Current			1	μA	V_{OUT} = 0V, T_A = 25°C
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}(2)	Supply Current During t_{PC}		37	56	mA	All Addresses = 0V Precharge = 0V Cenable = V_{SS}; T_A = 25°C
I_{DD2}(2)	Supply Current During t_{OV}		38	59	mA	All Addresses = 0V Precharge = 0V Cenable = 0V; T_A = 25°C
I_{DD3}(2)	Supply Current During t_{POV}		5.5	11	mA	Precharge = V_{SS} Cenable = 0V; T_A = 25°C
I_{DD4}(2)	Supply Current During t_{CP}		3	4	mA	Precharge = V_{SS} Cenable = V_{SS}; T_A = 25°C
I_{DD}(5)AV	Average Supply Current		17	25	mA	Cycle Time = 580 ns; Precharge Width = 190 ns; T_A = 25°C
V_{IL1}(7)	Input Low Voltage (All Address & Data-in Lines)	V_{SS}−17		V_{SS}−14.2	V	T_A = 0°C
V_{IL2}(7)	Input Low Voltage (All Address & Data-in Lines)	V_{SS}−17		V_{SS}−14.5	V	T_A = 70°C
V_{IL3}(7,8)	Input Low Voltage (Precharge Cenable & Read/Write Inputs)	V_{SS}−17		V_{SS}−14.7	V	T_A = 0°C
V_{IL4}(7,8)	Input Low Voltage (Precharge Cenable & Read/Write Inputs)	V_{SS}−17		V_{SS}−15.0	V	T_A = 70°C
V_{IH1}(7)	Input High Voltage (All Inputs)	V_{SS}−1		V_{SS}+1	V	T_A = 0°C
V_{IH2}(7)	Input High Voltage (All Inputs)	V_{SS}−0.7		V_{SS}+1	V	T_A = 70°C
I_{OH1}	Output High Current	600	900	4000	μA	T_A = 25°C, R_{LOAD} = 100Ω(4)
I_{OH2}	Output High Current	500	800	4000	μA	T_A = 70°C, R_{LOAD} = 100Ω(4)
I_{OL}	Output Low Current	See Note 3				R_{LOAD} = 100Ω(4)
V_{OH1}	Output High Voltage	60	90	400	mV	T_A = 25°C, R_{LOAD} = 100Ω(4)
V_{OH2}	Output High Voltage	50	80	400	mV	T_A = 70°C, R_{LOAD} = 100Ω(4)
V_{OL}	Output Low Voltage	See Note 3				

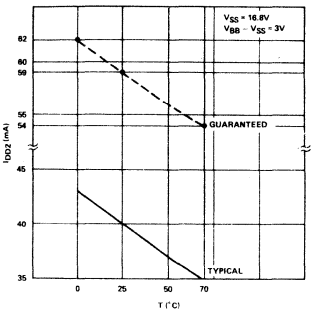
NOTES

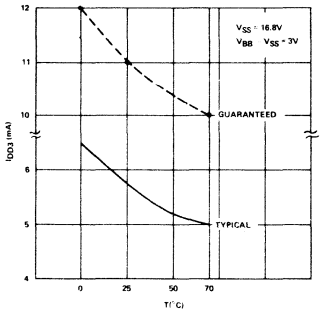
1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
2. See Supply Current vs. Temperature (p. 3) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.
5. This parameter is periodically sampled and is not 100% tested.
6. (V_{BB} − V_{SS}) supply should be applied at or before V_{SS}.
7. The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C. Thus any value between 0°C and 70°C can be calculated using a straight-line relationship.
8. The maximum values for V_{IL} (for precharge, cenable & read/write) may be increased to V_{SS}−14.2 @ 0°C and V_{SS} −14.5 @ 70°C (same values as those specified for the address and data-in lines) with a 40 ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

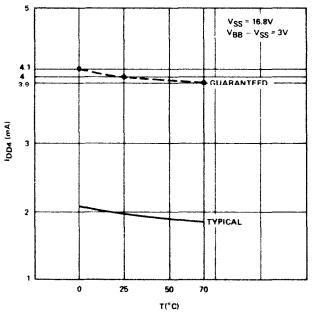
CHARACTERISTIC CURVES

SUPPLY CURRENT VS TEMPERATURE

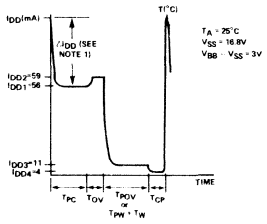








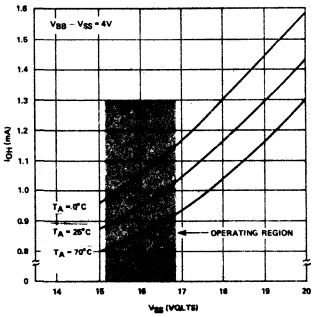
I_{DD} VS TIME

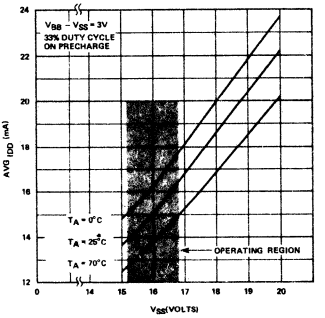


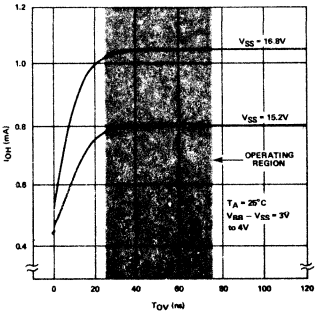
NOTES:

1. ΔI_{DD} is due to charging of internal device node capacitance at precharge.
2. These values are taken from a single pulse measurement.

CHARACTERISTIC CURVES (Cont'd)







AC CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{SS} = 16 \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0$

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	Time Between Refresh			2	ms	
t_{AC}(1)	Address to Cenable Set Up Time	115			ns	
t_{CA}	Cenable to Address Hold Time	20			ns	
t_{PC}(1)	Precharge to Cenable Delay	125			ns	
t_{OVL}	Precharge & Cenable Overlap, Low	25		75	ns	
t_{CP}	Cenable to Precharge Delay	85			ns	
t_{OVH}	Precharge & Cenable Overlap, High			140	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC}(1)	Read Cycle	480			ns	
t_{POV}	Precharge to End of Cenable	165		500	ns	
t_{PO}	End of Precharge to Output Delay			120	ns	$t_T = 20$ ns
t_{ACC1}(1)	Address to Output Access	300			ns	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2t_T$; $C_{LOAD} = 100$ pF, $R_{LOAD} = 100\Omega$, $V_{REF} = 40$ mV
t_{ACC2}(1)	Precharge to Output Access	310			ns	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2t_T$; $C_{LOAD} = 100$ pF, $R_{LOAD} = 100\Omega$, $V_{REF} = 40$ mV

AC CHARACTERISTICS (Cont'd)

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}(1)	Write Cycle	580			ns	t_T = 20 ns
t_{RWC}(1)	Read/Write Cycle	580			ns	
t_{PW}	Precharge to Read/Write Delay	165		500	ns	
t_{WP}	Read/Write Pulse Width	50			ns	
t_W	Read/Write Set Up Time	80			ns	
t_{DW}	Data Set Up Time	105			ns	
t_{DH}	Data Hold Time	10			ns	
t_{PO}	End of Precharge to Output Delay			120	ns	C_{LOAD} = 100 pF R_{LOAD} = 100Ω V_{REF} = 40 mV
t_P	Time to Next Precharge	0			ns	
t_{CW}	Read/Write Hold Time			10	ns	

CAPACITANCE (note 2)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
C_{AD}	Address Capacitance		5	7	pF	V_{IN} = V_{SS}
C_{PR}	Precharge Capacitance		15	18	pF	V_{IN} = V_{SS}
C_{CE}	Cenable Capacitance		15	18	pF	V_{IN} = V_{SS}
C_{RW}	Read/Write Capacitance		11	15	pF	V_{IN} = V_{SS}
C_{IN1}	Data Input Capacitance		4	5	pF	Cenable = 0V V_{IN} = V_{SS}
C_{IN2}	Data Input Capacitance		2	4	pF	Cenable = V_{SS} V_{IN} = V_{SS}
C_{OUT}	Data Output Capacitance		2	3	pF	V_{OUT} = 0V

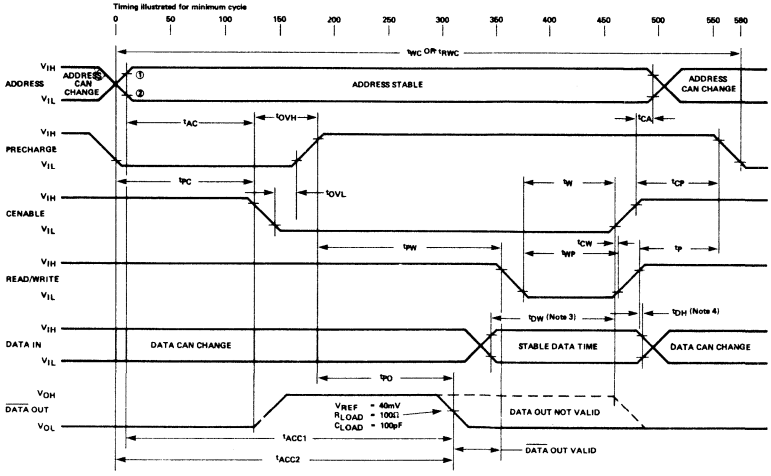
f = 1 MHz
All Unused Pins are at A.C. Ground

(1) These times will degrade by 40 ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS} – 14.2V @ 0°C and V_{SS}–14.5V @ 70°C as defined on page 2.

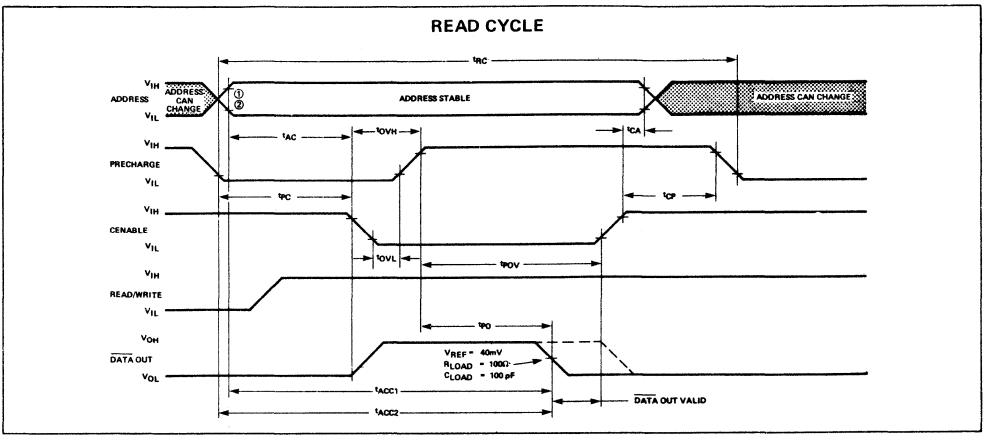
(2) This parameter is periodically sampled and is not 100% tested. It is measured at worst case operating conditions. Capacitance measurements for plastic packages only.

TIMING DIAGRAM

WRITE CYCLE OR READ/WRITE CYCLE



TIMING DIAGRAM (Cont'd)



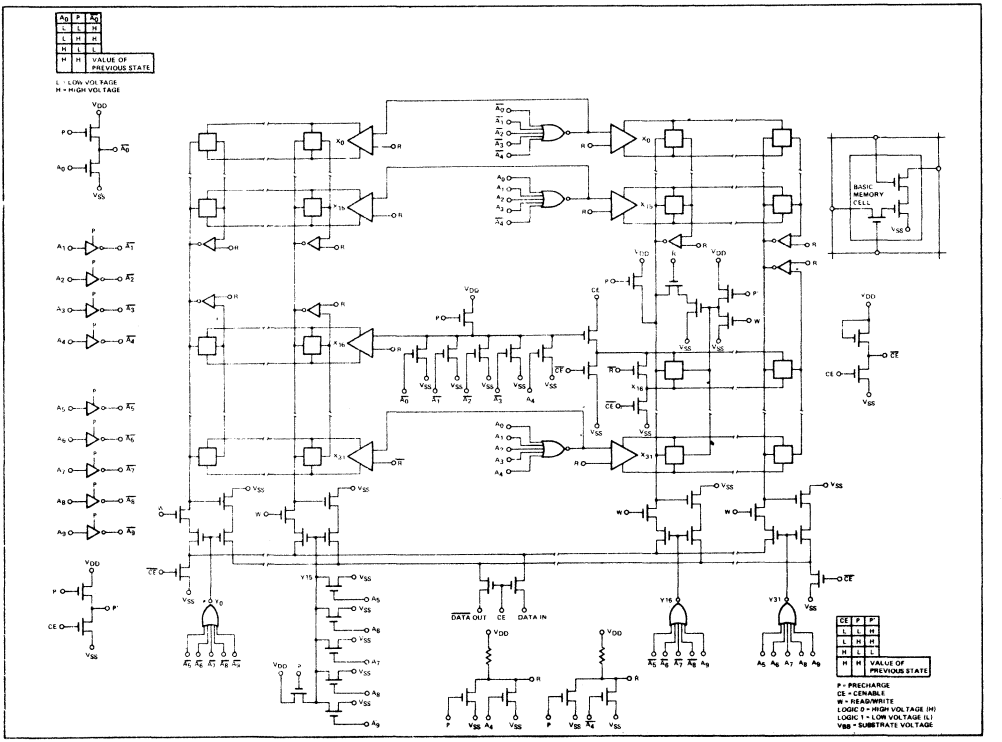
NOTES:

① $V_{DD} + 2V$
② $V_{SS} - 2V$
t_T is defined as the transitions between these two points.

3 t_{DW} is referenced to point ② of the rising edge of cenable or read/write whichever occurs first.

4 t_{DH} is referenced to point ① of the rising edge of cenable or read/write whichever occurs first.

CIRCUIT SCHEMATIC



signetics

1024-BIT RANDOM ACCESS READ/WRITE DYNAMIC MEMORY (HIGH SPEED VERSION) 1103-1

SILICON GATE MOS

DESCRIPTION

The Signetics 1103-1 is designed for main memory applications where high performance, low cost and large bit storage are important design objectives. It is a 1024 word by 1 bit random access memory element using enhancement mode P-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18-pin dual in-line package. The dynamic circuitry dissipates significant power only during precharge. Information stored in the memory is nondestructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds. A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied. Use Signetics 8T28 Sense Amp, and 3207 Clock Driver.

FEATURES

- LOW POWER DISSIPATION – DISSIPATES POWER PRIMARILY ON SELECTED CHIPS
- ACCESS TIME – 150 nsec.
- CYCLE TIME – 340 nsec.
- REFRESH PERIOD – 1 MILLISECOND FOR 0-55°C AMBIENT
- OR-TIE CAPABILITY
- SIMPLE MEMORY EXPANSION WITH CHIP ENABLE
- FULLY DECODED – ON-CHIP ADDRESS DECODE
- INPUTS PROTECTED – ALL INPUTS HAVE PROTECTION AGAINST STATIC CHARGE
- LOW COST PACKAGING – 18 PIN SILICONE AND 18 PIN CERAMIC DUAL IN-LINE

APPLICATIONS

CORE MEMORY REPLACEMENT
BUFFER STORES
MAIN MEMORY

PROCESS TECHNOLOGY

The use of Signetics' unique silicon gate low threshold process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

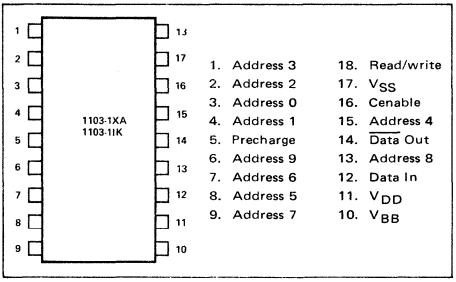
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric

SILICONE PACKAGING (Cont'd)

material over the silicon gate-oxide substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

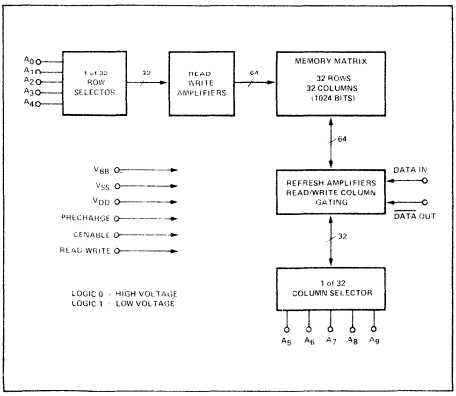
PIN CONFIGURATION (Top View)



PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP RANGE
1103-1XA	18-Pin DIP Silicone	0–55°C
1103-1IK	18-Pin DIP Ceramic	0–55°C

BLOCK DIAGRAM



AC CHARACTERISTICS $T_A = 0°C$ to $+55°C$; $V_{SS} = 19 \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	Time Between Refresh			1	ms	
t_{AC}	Address to Cenable Set Up Time	30			ns	
t_{CA}	Cenable to Address Hold Time	10			ns	
t_{PC}	Precharge to Cenable Delay	60			ns	
t_{OVL}	Precharge & Cenable Overlap, Low	5		30	ns	
t_{CP}	Cenable to Precharge Delay	40			ns	
t_{OVH}	Precharge & Cenable Overlap, High			85	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC}(1)	Read Cycle	300			ns	
t_{POV}	Precharge to End of Cenable	115		500	ns	
t_{PO}(1)	End of Precharge to Output Delay			75	ns	$t_T = 20$ ns
t_{ACC1}(1)	Address to Output Access	150			ns	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2t_T$; $C_{LOAD} = 50$ pF; $R_{LOAD} = 100\Omega$
t_{ACC2}(1)	Precharge to Output Access	180			ns	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2t_T$; $V_{REF} = 80$ mV

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}	Write Cycle	340			ns	$t_T = 20$ ns
t_{RWC}(1)	Read/Write Cycle	340			ns	
t_{PW}	Precharge to Read/Write Delay	115		500	ns	
t_{WP}	Read/Write Pulse Width	20			ns	
t_W	Read/Write Set Up Time	20			ns	
t_{DW}	Data Set Up Time	40			ns	
t_{DH}	Data Hold Time	10			ns	
t_{PO}(1)	End of Precharge to Output Delay			75	ns	$C_{LOAD} = 50$ pF; $R_{LOAD} = 100\Omega$; $V_{REF} = 80$ mV
t_P	Time to Next Precharge	0			ns	
t_{CW}	Read/Write Hold Time			15	ns	

CAPACITANCE (note 2)

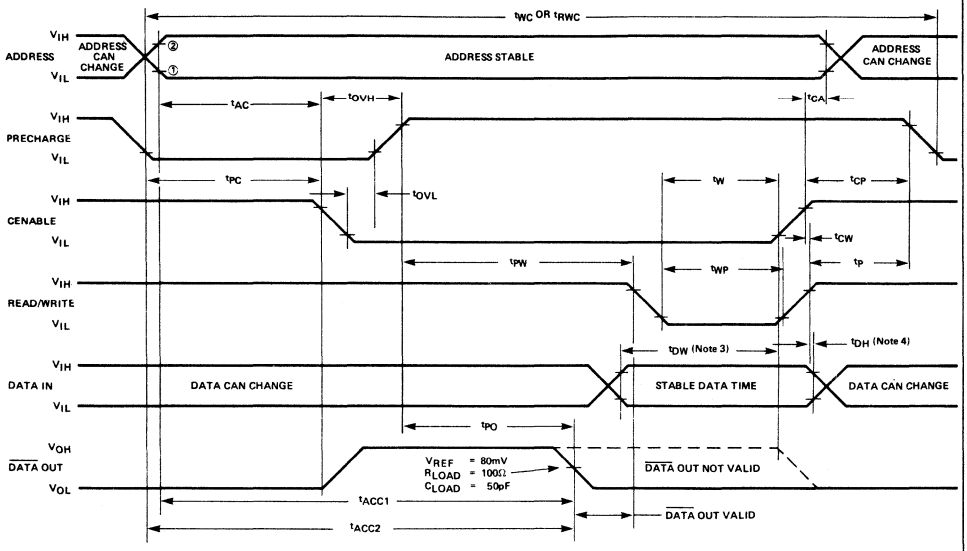
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
C_{AD}	Address Capacitance		5	7	pF	$V_{IN} = V_{SS}$; f = 1 MHz; All Unused Pins are at A.C. Ground
C_{PR}	Precharge Capacitance		15	18	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance		15	18	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance		11	15	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance		4	5	pF	Cenable = 0V; $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance		2	4	pF	Cenable = V_{SS}; $V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance		2	3	pF	$V_{OUT} = 0V$

(1) These times will degrade by 35 ns if a V_{REF} point of 40 mV is chosen instead of the 80 mV point defined in this specification.

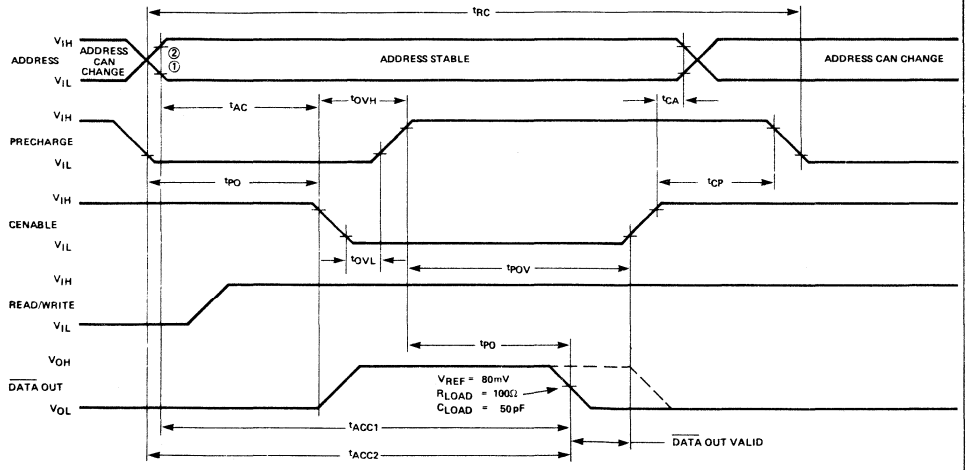
(2) This parameter is periodically sampled and is not 100% tested. It is measured at worst case operating conditions. Capacitance measurements for plastic packages only.

TIMING DIAGRAM

WRITE CYCLE OR READ/WRITE CYCLE



READ CYCLE



NOTES:

① V_{DD} + 2V
② V_{SS} - 2V
t_T is defined as the transitions between these two points.

3 t_{DW} is referenced to point ① of the rising edge of cenable or read/write whichever occurs first.

4 t_{DH} is referenced to point ② of the rising edge of cenable or read/write whichever occurs first.

MAXIMUM GUARANTEED RATINGS [8]

Operating Ambient Temperature	0°C to 55°C	Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to +0.8V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.0W
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{BB}	−25V to +0.8V		

D.C. AND OPERATING CHARACTERISTICS

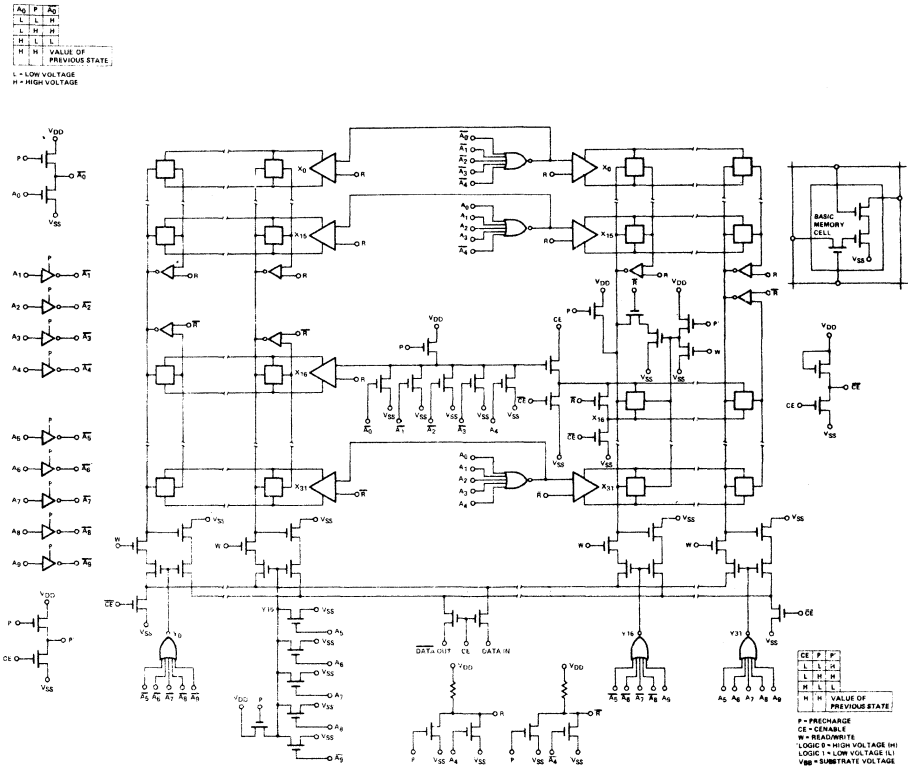
T_A = 0°C to +55°C, V_{SS}[1] = 19V ± 5%, ($V_{BB} - V_{SS}$)[6] = 3V to 4V, V_{DD} = 0V unless otherwise specified (Note 7).

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All input pins)			10	μA	V_{IN} = 0V, T_A = 25°C
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V, T_A = 25°C
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}[2]	Supply Current During t_{PC}		45	60	mA	All Addresses = 0V Precharge = 0V Cenable = V_{SS}; T_A = 25°C
I_{DD2}[2]	Supply Current During τ_{0V}		50	68.5	mA	All addresses = 0V Precharge = 0V Cenable = 0V; T_A = 25°C
I_{DD3}[2]	Supply Current During t_{POV}		8.5	11	mA	Precharge = V_{SS} Cenable = 0V; T_A = 25°C
I_{DD4}[2]	Supply Current During t_{CP}		3	4	mA	Precharge = V_{SS} Cenable = V_{SS}; T_A = 25°C
I_{DD}[5]AV	Average Supply Current		20	23	mA	Precharge Width =105ns @ 50% Cycle Time = 340 ns; T_A = 25°C
V_{IL1}	Input Low Voltage (All address and data-in lines)	V_{SS}−20		V_{SS}−17	V	
V_{IH1}	Input High Voltage (All Inputs)	V_{SS}−1		V_{SS}+1	V	
I_{OH1}	Output High Current	1.15	1.3	7.0	mA	T_A = 25°C, R_{LOAD} = 100Ω[4]
I_{OH2}	Output High Current	0.9	1.15	7.0	mA	T_A = 55°C, R_{LOAD} = 100Ω[4]
I_{OL}	Output Low Current	See Note 3				R_{LOAD} = 100Ω[4]
V_{OH1}	Output High Voltage	115	130	700	mV	T_A = 25°C, R_{LOAD} = 100Ω[4]
V_{OH2}	Output High Voltage	90	115	700	mV	T_A = 55°C, R_{LOAD} = 100Ω[4]
V_{OL}	Output Low Voltage	See Note 3				

NOTES:

1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
2. See Supply Current vs. Temperature (p. 3) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.
3. The output current when reading a low output is the leakage current of the 1103-1 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.
5. This parameter is periodically sampled and is not 100% tested.
6. ($V_{BB} - V_{SS}$) supply should be applied at or before V_{SS}.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CIRCUIT SCHEMATIC



signetics

2102 FAMILY OF 1024–BIT RANDOM ACCESS READ WRITE STATIC MEMORY

INCLUDES: 2102, 21L02, 21F02 AND M2102 SERIES

DESCRIPTION

The Signetics 2102 is a static random access read/write memory offering a 1024x1 organization. Fabricated with low threshold N-Channel silicon gate technology.

The 2102 is fully static, requiring no clocks and is completely DTL/TTL compatible including the single +5V power supply requirement.

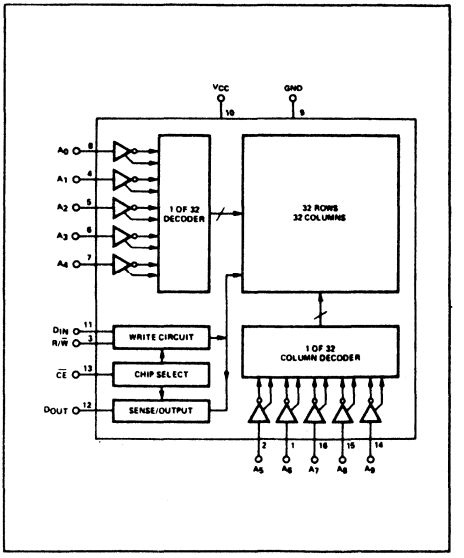
FEATURES

- 1024x1 ORGANIZATION
- COMPLETELY STATIC OPERATION
- +5V POWER SUPPLY ONLY
- TTL COMPATIBLE INPUTS
- THREE-STATE TTL OUTPUT
- 16-PIN DIP PACKAGE
- 200 mW DISSIPATION TYPICAL
- N-CHANNEL SILICON GATE
- NO CLOCKS, NO REFRESHING, NO SENSING

APPLICATIONS

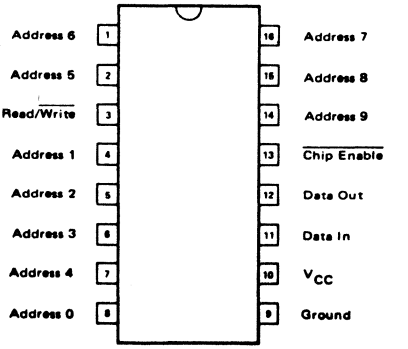
PERIPHERAL MEMORIES
BUFFER MEMORIES
MINICOMPUTER MEMORY

BLOCK DIAGRAM



PIN CONFIGURATION

B PACKAGE



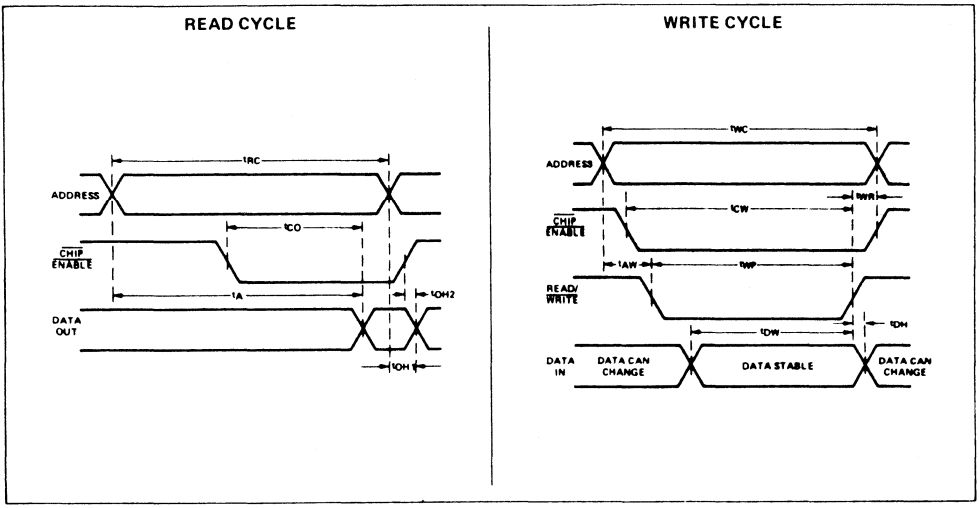
MAXIMUM GUARANTEED RATINGS(1)

Storage Temperature	−65°C to +150°C
All Input, Output and Supply Voltages with respect to Ground	−0.5V to +7V
Package Power Dissipation(2)	
"B" Package	640 mW
"F" Package	1 Watt
"I" Package	1 Watt

PART IDENTIFICATION

TYPE	PACKAGE	t_{ACCESS}	OP TEMP. RANGE
2102-2B	16-Pin Plastic DIP	650ns	0-70°C

TIMING DIAGRAMS



A.C. CONDITIONS OF TEST

Input Pulse Levels:	+0.65 Volt to +2.2 Volt
Input Pulse Rise and Fall Times:	20 ns
Timing Measurement Reference Level:	1.5 Volt
Output Load:	1 TTL Gate and C_L = 100 pF

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient ("B" package).
3. All inputs protected against static charge.
4. Parameter valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.

A. C. Characteristics 2102-1 (500 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	500			ns
t_A	Access time			500	ns
t_{CO}	Chip enable to output time			350	ns
t_{OH1}	Previous read data valid with respect to address	50			ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	500			ns
t_{AW}	Address to write setup time	150			ns
t_{WP}	Write pulse width	300			ns
t_{WR}	Write recovery time	50			ns
t_{DW}	Data setup time	330			ns
t_{DH}	Data hold time	100			ns
t_{CW}	Chip enable to write setup time	400			ns

A. C. Characteristics 2102-2 (650 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	650			ns
t_A	Access time			650	ns
t_{CO}	Chip enable to output time			400	ns
t_{OH1}	Previous read data valid with respect to address	50			ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	650			ns
t_{AW}	Address to write setup time	200			ns
t_{WP}	Write pulse width	400			ns
t_{WR}	Write recovery time	50			ns
t_{DW}	Data setup time	450			ns
t_{DH}	Data hold time	100			ns
t_{CW}	Chip enable to write setup time	550			ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

D. C. and Operating Characteristics for 2102, 2102-1, 2102-2

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input load current (All input pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output leakage current			10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output leakage current			−100	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power supply current		30	60	mA	All inputs = 5.25V Data out open T_A = 25°C
I_{CC2}	Power supply current			70	mA	All inputs = 5.25V Data out open T_A = 0°C
V_{IL}	Input "low" voltage	−0.5		+0.65	V	
V_{IH}	Input "high" voltage	2.2		V_{CC}	V	
V_{OL}	Output "low" voltage			+0.45	V	I_{OL} = 1.9 mA
V_{OH}	Output "high" voltage	2.2			V	I_{OH} = −100 μA

A. C. Characteristics 2102 (1000 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	1000			ns
t_A	Access time		500	1000	ns
t_{CO}	Chip enable to output time			500	ns
t_{OH1}	Previous read data valid with respect to address	50			ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	1000			ns
t_{AW}	Address to write setup time	200			ns
t_{WP}	Write pulse width	750			ns
t_{WR}	Write recovery time	50			ns
t_{DW}	Data setup time	800			ns
t_{DH}	Data hold time	100			ns
t_{CW}	Chip enable to write setup time	900			ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

D. C. and Operating Characteristics for 21L02, 21L02-1, 21L02-2, 21L02-3

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input load current (All input pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output leakage current			10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output leakage current			−100	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power supply current		30	40	mA	All inputs = 5.25V Data out open T_A = 25°C
I_{CC2}	Power supply current			40	mA	All inputs = 5.25V Data out open T_A = 0°C
V_{IL}	Input "low" voltage	−0.5		+0.65	V	
V_{IH}	Input "high" voltage	2.2		V_{CC}	V	
V_{OL}	Output "low" voltage			+0.45	V	I_{OL} = 1.9 mA
V_{OH}	Output "high" voltage	2.2			V	I_{OH} = −100 μA

A. C. Characteristics 21L02 (1000 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	1000			ns
t_A	Access time		500	1000	ns
t_{CO}	Chip enable to output time			500	ns
t_{OH1}	Previous read data valid with respect to address	50			ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	1000			ns
t_{AW}	Address to write setup time	200			ns
t_{WP}	Write pulse width	750			ns
t_{WR}	Write recovery time	50			ns
t_{DW}	Data setup time	800			ns
t_{DH}	Data hold time	100			ns
t_{CW}	Chip enable to write setup time	900			ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics 21L02-1 (500 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	500			ns
t_A	Access time			500	ns
t_{CO}	Chip enable to output time			350	ns
t_{OH1}	Previous read data valid with respect to address	50			ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	500			ns
t_{AW}	Address to write setup time	150			ns
t_{WP}	Write pulse width	300			ns
t_{WR}	Write recovery time	50			ns
t_{DW}	Data setup time	330			ns
t_{DH}	Data hold time	100			ns
t_{CW}	Chip enable to write setup time	400			ns

A. C. Characteristics 21L02-2 (650 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	650			ns
t_A	Access time			650	ns
t_{CO}	Chip enable to output time			400	ns
t_{OH1}	Previous read data valid with respect to address	50			ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	650			ns
t_{AW}	Address to write setup time	200			ns
t_{WP}	Write pulse width	400			ns
t_{WR}	Write recovery time	50			ns
t_{DW}	Data setup time	450			ns
t_{DH}	Data hold time	100			ns
t_{CW}	Chip enable to write setup time	550			ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics 21L02-3 (400 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	400			ns
t_A	Access time			400	ns
t_{CO}	Chip enable to output time			300	ns
t_{OH1}	Previous read data valid with respect to address	50			ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	400			ns
t_{AW}	Address to write setup time	100			ns
t_{WP}	Write pulse width	250			ns
t_{WR}	Write recovery time	50			ns
t_{DW}	Data setup time	300			ns
t_{DH}	Data hold time	50			ns
t_{CW}	Chip enable to write setup time	300			ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

21F02 FAST SERIES

DESCRIPTION

Signetics 21F02 is a high speed 1024 word by one bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 21F02 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Signetics 21F02 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

D. C. and Operating Characteristics for 21F02, 21F02-2, 21F02-4

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input load current (All input pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output leakage current			5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Output leakage current			−10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC1}	Power supply current		30	60	mA	All inputs = 5.25V Data out open T_A = 25°C
I_{CC2}	Power supply current			70	mA	All inputs = 5.25V Data out open T_A = 0°C
V_{IL}	Input "low" voltage	−0.5		0.8	V	
V_{IH}	Input "high" voltage	2.0		V_{CC}	V	
V_{OL}	Output "low" voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output "high" voltage	2.4			V	I_{OH} = −100 μA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics 21F02 (350 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	350			ns
t_A	Access time			350	ns
t_{CO}	Chip enable to output time		180		ns
t_{OH1}	Previous read data valid with respect to address		40		ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	350			ns
t_{AW}	Address to write setup time		20		ns
t_{WP}	Write pulse width		250		ns
t_{WR}	Write recovery time		20		ns
t_{DW}	Data setup time		250		ns
t_{DH}	Data hold time	0			ns
t_{CW}	Chip enable to write setup time		250		ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics 21F02-2 (250 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	250			ns
t_A	Access time			250	ns
t_{CO}	Chip enable to output time		130		ns
t_{OH1}	Previous read data valid with respect to address		40		ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	250			ns
t_{AW}	Address to write setup time		20		ns
t_{WP}	Write pulse width		180		ns
t_{WR}	Write recovery time		20		ns
t_{DW}	Data setup time		180		ns
t_{DH}	Data hold time	0			ns
t_{CW}	Chip enable to write setup time		180		ns

A. C. Characteristics 21F02-4 (450 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	450			ns
t_A	Access time			450	ns
t_{CO}	Chip enable to output time		230		ns
t_{OH1}	Previous read data valid with respect to address		40		ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	450			ns
t_{AW}	Address to write setup time		20		ns
t_{WP}	Write pulse width		300		ns
t_{WR}	Write recovery time		20		ns
t_{DW}	Data setup time		300		ns
t_{DH}	Data hold time	0			ns
t_{CW}	Chip enable to write setup time		300		ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

D. C. and Operating Characteristics

$T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input load current (All input pins)			10	μA	V_{IN} = 0 to 5.5V
I_{LOH}	Output leakage current			10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.2 to V_{CC}
I_{LOL}	Output leakage current			−50	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.45V
I_{CC1}	Power supply current		30	60	mA	All inputs = 5.5V Data out open $T_A = 25°C$
I_{CC2}	Power supply current			70	mA	All inputs = 5.5V Data out open $T_A = -55°C$
V_{IL}	Input "low" voltage	−0.5		0.8	V	
V_{IH}	Input "high" voltage	2.0		V_{CC}	V	
V_{OL}	Output "low" voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output "high" voltage	2.2			V	I_{OH} = −100 μA

A. C. Characteristics M2102-4 (450 ns Cycle Time)

$T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	450			ns
t_A	Access time			450	ns
t_{CO}	Chip enable to output time		230		ns
t_{OH1}	Previous read data valid with respect to address		40		ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	450			ns
t_{AW}	Address to write setup time		20		ns
t_{WP}	Write pulse width		300		ns
t_{WR}	Write recovery time		20		ns
t_{DW}	Data setup time		300		ns
t_{DH}	Data hold time	0			ns
t_{CW}	Chip enable to write setup time		300		ns

NOTE 1 Typical values are for $T_A = 25°C$ and nominal supply voltage.

M2102-6 MILITARY SERIES

D. C. and Operating Characteristics

$T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input load current (All input pins)			10	μA	V_{IN} = 0 to 5.5V
I_{LOH}	Output leakage current			10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output leakage current			−100	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power supply current		30	60	mA	All inputs = 5.5V Data out open $T_A = 25°C$
I_{CC2}	Power supply current			70	mA	All inputs = 5.5V Data out open $T_A = -55°C$
V_{IL}	Input "low" voltage	−0.5		+0.65	V	
V_{IH}	Input "high" voltage	2.2		V_{CC}	V	
V_{OL}	Output "low" voltage			+0.45	V	I_{OL} 1.9 mA
V_{OH}	Output "high" voltage	2.2			V	$I_{OH} = -100\,\mu A$

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage

A. C. Characteristics M2102-6 (650 ns Cycle Time)

$T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
READ CYCLE					
t_{RC}	Read cycle	650			ns
t_A	Access time			650	ns
t_{CO}	Chip enable to output time		400		ns
t_{OH1}	Previous read data valid with respect to address		50		ns
t_{OH2}	Previous read data valid with respect to chip enable	0			ns
WRITE CYCLE					
t_{WC}	Write cycle	650			ns
t_{AW}	Address to write setup time		200		ns
t_{WP}	Write pulse width		400		ns
t_{WR}	Write recovery time		50		ns
t_{DW}	Data setup time		450		ns
t_{DH}	Data hold time		100		ns
t_{CW}	Chip enable to write setup time		550		ns

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage

signetics

2606 FAMILY OF 256X4 RANDOM ACCESS READ WRITE STATIC MEMORY

PRELIMINARY SPECIFICATIONS

N CHANNEL SILICON GATE MOS 2600 SERIES

DESCRIPTION

Signetics' 2606 is a fully decoded, static, read/write, random access memory. It has a capacity of 1024-bits and is organized as 256 x 4. The 2606 is fabricated with N-Channel silicon gate MOS technology and achieves an access time of less than 750 nanoseconds. No clocks are required and all interface signals are directly TTL compatible including the power supply.

FEATURES

- 256 x 4 ORGANIZATION
- STATIC OPERATION
- 750ns ACCESS TIME
- 750ns CYCLE TIME
- SINGLE 5 VOLT POWER SUPPLY
- TTL COMPATIBLE INPUTS AND OUTPUTS
- 200mW TYPICAL POWER DISSIPATION
- MULTIPLEXED DATA BUS
- TRI-STATE OUTPUTS
- N-CHANNEL SILICON GATE TECHNOLOGY
- STANDARD 300-MIL 16 PIN PACKAGE

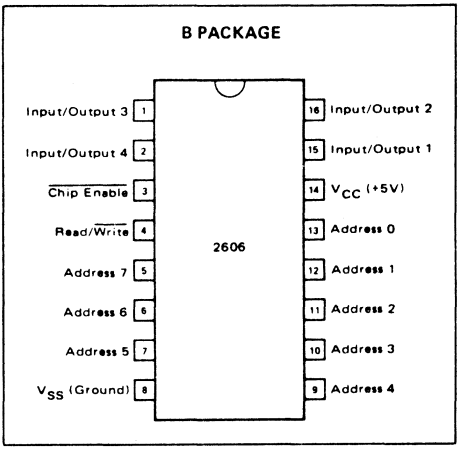
APPLICATIONS

MICROCOMPUTER MEMORIES
PERIPHERAL DEVICES
TERMINALS
DATA BUFFERS

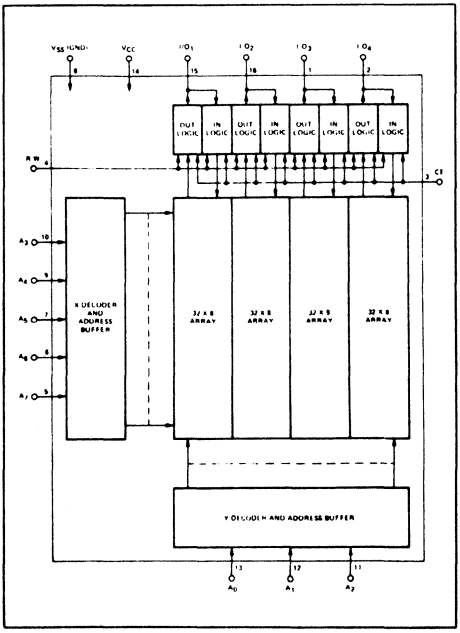
MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input, Output, and Supply Voltages with respect to ground pin(3)	−0.5V to +6V
Package Power Dissipation(2)	
"B" Package	640 mW
"F" Package	1 Watt
"I" Package	1 Watt

PIN CONFIGURATION



BLOCK DIAGRAM



D. C. Operating Characteristics for 2606 and 2606-1

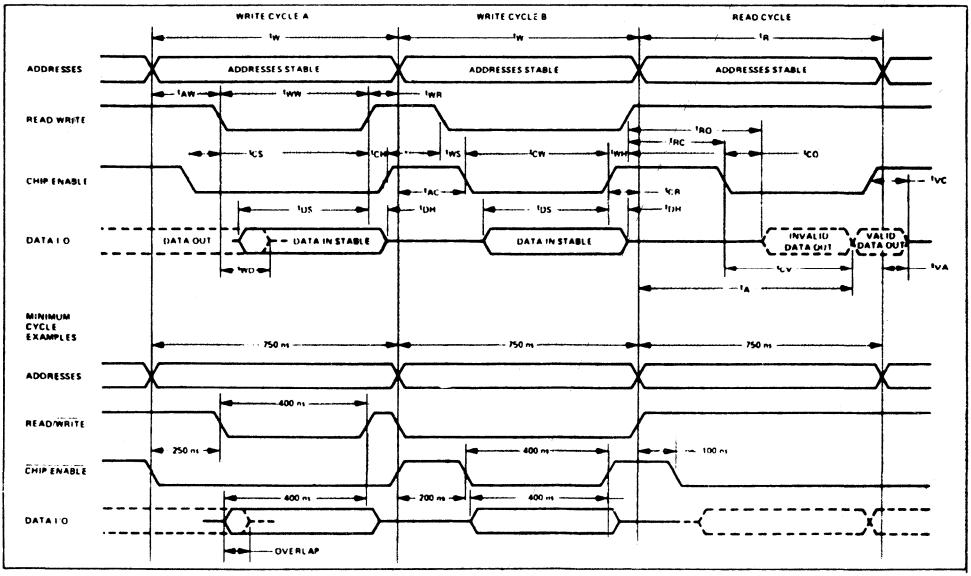
T_A = 0°C to +70°C, V_{CC} = +5V ±5% unless otherwise specified. See Notes 3, 4, 5, 6 and 7.

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
I_{LI}	Input load current			10	μA	V_{IN} = 0 to 5.25V
I_{BH}	Bus high current			10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{BL}	Bus low current			−100	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC}	Power supply current		40	70 80	mA mA	All inputs = 5.25V Data bus open T_A = 25°C T_A = 0°C
V_{IL}	Input low voltage	−0.5		+0.65	V	
V_{IH}	Input high voltage	2.2		V_{CC}	V	
V_{OL}	Output low voltage			+0.45	V	I_{OL} = 1.9 mA
V_{OH}	Output high voltage	2.4			V	I_{OH} = −100 μA
C_{IN}	Input capacitance		4	7	pF	V_{IN} = 0V
$C_{I/O}$	Data bus capacitance		7	10	pF	V_{OUT} = 0V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150 C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient ("B" package).
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameter valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make a design and process changes and improvements.
7. Typical values are at +25°C, nominal supply voltages, and nominal processing parameters.

TIMING DIAGRAM



A. C. Operating Characteristics 2606-1 (500 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = +5V ±5% unless otherwise specified. See Notes E, F, G & H.

WRITE CYCLE A		MIN.	MAX.	UNITS	NOTES
t_{AW}	Address to write time	150		ns	
t_{WW}	Write pulse width	300		ns	
t_{WR}	Write recovery time	50		ns	
t_{CS}	Chip enable set-up	0		ns	
t_{CH}	Chip enable hold	0		ns	
t_{DS}	Data in set-up	280		ns	
t_{DH}	Data in hold	0		ns	NOTE A
t_{WD}	Write to data out disable delay		100	ns	NOTE D
t_W	Write cycle time	500		ns	
WRITE CYCLE B					
t_{AC}	Address to chip enable time	150		ns	
t_{CW}	Chip enable pulse width	300		ns	
t_{CR}	Chip enable recovery time	50		ns	
t_{WS}	Write set-up	100		ns	NOTE B
t_{WH}	Write hold	0		ns	
t_{DS}	Data in set-up	280		ns	
t_{DH}	Data in hold	0		ns	NOTE A
t_W	Write cycle time	500		ns	
READ CYCLE					
t_R	Read cycle time	500		ns	
t_A	Access time		500	ns	
t_{RO}	Read to output enabled	75		ns	NOTE C
t_{CO}	Chip enable to output enable	0		ns	NOTE C
t_{VC}	Previous data valid with respect to chip disable	0	100	ns	
t_{VA}	Previous data valid with respect to address change	50		ns	
t_{CV}	Chip enable to data valid delay		300	ns	
t_{RC}	Read to chip enable	50		ns	

NOTES

A. Maximum t_{DH} governed by potential conflict with data out during next cycle.
B. Write set-up required to prevent data overlap. For write cycle B the R/$\overline{W}$ line will typically change with the addresses.
C. R/$\overline{W}$ must be high and $\overline{CE}$ must be low in order for output buffers to turn on.
D. The output buffers will turn off within the specified time after write mode is selected.
E. Input levels swing between 0.65 volt and 2.2 volts.
F. Input signal transition times are 20 ns.
G. Timing reference level is 1.5 volts.
H. Bus load is 100 pF, one TTL input and one TTL tristate output.

A. C. Operating Characteristics 2606-1 (500 ns Cycle Time)

T_A = 0°C to 70°C, V_{CC} = +5V ±5% unless otherwise specified. See Notes E, F, G & H.

WRITE CYCLE A		MIN.	MAX.	UNITS	NOTES
t_{AW}	Address to write time	150		ns	
t_{WW}	Write pulse width	300		ns	
t_{WR}	Write recovery time	50		ns	
t_{CS}	Chip enable set-up	0		ns	
t_{CH}	Chip enable hold	0		ns	
t_{DS}	Data in set-up	280		ns	
t_{DH}	Data in hold	0		ns	NOTE A
t_{WD}	Write to data out disable delay		100	ns	NOTE D
t_W	Write cycle time	500		ns	
WRITE CYCLE B					
t_{AC}	Address to chip enable time	150		ns	
t_{CW}	Chip enable pulse width	300		ns	
t_{CR}	Chip enable recovery time	50		ns	
t_{WS}	Write set-up	100		ns	NOTE B
t_{WH}	Write hold	0		ns	
t_{DS}	Data in set-up	280		ns	
t_{DH}	Data in hold	0		ns	NOTE A
t_W	Write cycle time	500		ns	
READ CYCLE					
t_R	Read cycle time	500		ns	
t_A	Access time		500	ns	
t_{RO}	Read to output enabled	75		ns	NOTE C
t_{CO}	Chip enable to output enable	0		ns	NOTE C
t_{VC}	Previous data valid with respect to chip disable	0	100	ns	
t_{VA}	Previous data valid with respect to address change	50		ns	
t_{CV}	Chip enable to data valid delay		300	ns	
t_{RC}	Read to chip enable	50		ns	

NOTES

A. Maximum t_{DH} governed by potential conflict with data out during next cycle.
B. Write set-up required to prevent data overlap. For write cycle B the R/$\overline{W}$ line will typically change with the addresses.
C. R/W must be high and $\overline{CE}$ must be low in order for output buffers to turn on.
D. The output buffers will turn off within the specified time after write mode is selected.
E. Input levels swing between 0.65 volt and 2.2 volts.
F. Input signal transition times are 20 ns.
G. Timing reference level is 1.5 volts.
H. Bus load is 100 pF, one TTL input and one TTL tristate output.

CIRCUIT FUNCTION DESCRIPTION

The Signetics 2606 is a 256 x 4 static, random access, read/write memory. It is divided into 4 arrays, each with 32 rows and 8 columns. Individual rows are selected by one of the thirty two decoders controlled by the A_3 through A_7 inputs. Individual columns are likewise selected by one of the eight column decoders controlled by the A_0 through A_2 inputs. During a read or write cycle, a cell from each of the four arrays will be selected. Thus, data is written into or read from the four arrays through the four I/O terminals in parallel. Once a cell is selected, its output is sensed by a differential amplifier which drives the tri-state output buffer. The output buffer is enabled by applying a high input at the R/$\overline{W}$ terminal and a low input at the $\overline{CE}$ terminal. New data is entered through the I/O terminals with both the $\overline{CE}$ and R/$\overline{W}$ terminals at the low state.

CHIP ENABLE

The $\overline{CE}$ affects both the R/$\overline{W}$ and I/O terminals. A write or read operation can take place only if the $\overline{CE}$ input is in the low state. When the $\overline{CE}$ input is in the high state, the output buffer is turned off and the input circuitry is disabled. The output buffer will be disabled less than 100ns after the CE input goes to a high state and will be enabled less than 150ns after the $\overline{CE}$ input goes to a low state.

READ/$\overline{WRITE}$ (R/$\overline{W}$)

Read and write operations are controlled by the R/$\overline{W}$ terminal for enabled chips. A low state on the R/$\overline{W}$ input selects the write mode and disables the tri-state output buffer. The output buffer will be disabled less than 100ns after the R/$\overline{W}$ input goes to a low state and will stay disabled for at least 75ns after the R/$\overline{W}$ input goes to a high state. A high state on the R/W input selects the read mode and disables the data input circuitry.

INPUT/OUTPUT (I/O)

The four I/O terminals are used for both input and output data transfer. In order to perform a minimum length write cycle with a timed read/write pulse (WRITE CYCLE A), there will be an overlap of the input and output data. This overlap occurs because in this mode the output buffer is controlled by the read/write line, and it does not turn off before input data is required. Input data must be able to dominate the bus. With the input and output data contending for control of the I/O bus, there can be large current spikes at the I/O terminals. The 2606 is designed to operate under these overlap conditions. The overlap can be avoided by extending the write cycle time to allow a delay in the data input. Alternatively, as shown in WRITE CYCLE B, the chip enable input can become the timed signal and the overlap is avoided with no sacrifice in cycle time. In this case the R/$\overline{W}$ line becomes an input level much like another address line.

signetics

4096-BIT READ/WRITE RANDOM ACCESS DYNAMIC MEMORY | 2604

PRELIMINARY SPECIFICATIONS

MOS 2600 SERIES

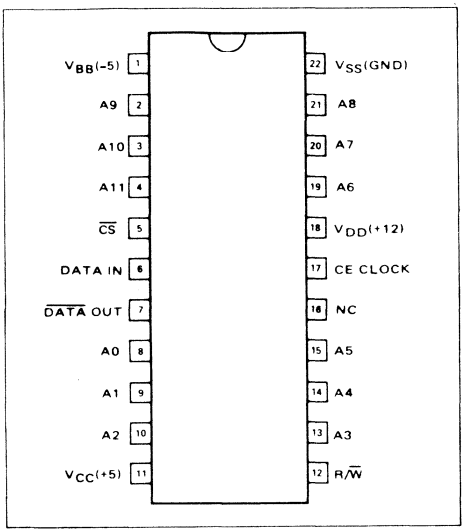
DESCRIPTION

Signetics 2604 is a high speed, fully decoded, dynamic, read/write, random access memory. It is organized as 4096X1 and achieves an access time of less than 300ns. All inputs except the CE Clock are fully TTL compatible and no special drivers or level shifters are required. The tri-state output buffers can drive 2 standard TTL loads.

The CE Clock is the only high level input required for the 2604. It is a low capacitance load and uses a nominal 12 volt signal swing. When the CE Clock goes low, internal signal nodes are pre-charged and the memory then assumes its standby mode and consumes very little power. All active operations are performed with the clock high.

The 2604 is a dynamic memory and each bit must be periodically refreshed. The internal organization allows refreshing to be accomplished by performing an operation at each of the 64 row addresses (derived from inputs A_0–A_5) every 2 milliseconds. The chip need not be selected during the refresh cycles.

PIN CONFIGURATION



FEATURES

- Capacity of 4096-bits
- Access time 300ns maximum
- Cycle time 470ns maximum
- Ion-implanted N-channel silicon gate MOS technology
- Standard supply voltages of +12, +5, -5 volts
- Single low capacitance high level clock input
- Address, control and data inputs fully TTL compatible
- Latches for address and control inputs provided on chip
- TTL tri-state output buffer
- Low power dissipation
- Standard 22-pin dual-in-line package

MAXIMUM GUARANTEED RATING*

Operating ambient temperature	0°C to +70°C
Storage temperature	-65°C to +150°C
All voltages with respect to V_{BB}	-0.3 to +20 volts

*Stresses above those listed may cause permanent damage to the device. These are stress ratings only and functional operation under these conditions is not implied.

PIN DESCRIPTION

Chip Enable Clock –

The master operating signal input is called the Chip Enable Clock. This signal is the only non-TTL-level input required to operate the 2604. Internal operations are executed while Chip Enable is in the "high" state. When Chip Enable is low, the 2604 is in the standby state (low power consumption) pre-charging internal nodes in preparation for the next memory cycle.

Chip Select –

The data in, data out, and read/write functions are all affected by the Chip Select input. Data is not accepted on the Data In terminal unless Chip Select and Read/Write are low. The write state of the Read/Write terminal is not recognized unless Chip Select is low. The output drivers are disconnected (tri-state) unless Chip Select has gone low at the appropriate time in a given cycle. Chip Select may be changed to the low state any time during a cycle as long as the correct write pulse timing is maintained. However, if Chip Select goes low more than 80 nsec into the cycle, the access time is lengthened accordingly. Chip Select may go high anytime after the minimum Chip Select pulse width requirement has been met. The chip remains selected for the remainder of the cycle. As with all other inputs to the 2604 except Chip Enable, Chip Select responds to a standard TTL-level signal without an external pull-up resistor.

PIN DISCRIPTION (cont.)

Read/$\overline{\text{Write}}$ –

Whether a given memory cycle is a read or a write cycle is determined by the Read/$\overline{\text{Write}}$ input. When Read/$\overline{\text{Write}}$ is high and the chip is selected, a read cycle is executed. When Read/$\overline{\text{Write}}$ is low and the chip is selected, a write cycle is executed. The internal write pulse width is determined by the falling edge of $\overline{\text{Chip Select}}$ or Read/$\overline{\text{Write}}$, whichever is later, and the trailing edge of Read/$\overline{\text{Write}}$.

Addresses –

All address inputs respond to TTL-level signals. The addresses in a given cycle must be stable before Chip Enable goes high. Addresses are latched on the 2604 so that the address inputs can change after the address hold time requirements have been met.

Data-in –

Input data is supplied to the 2604 on the Data-in terminal. This TTL-compatible input is used during a write cycle or read-modify-write cycle.

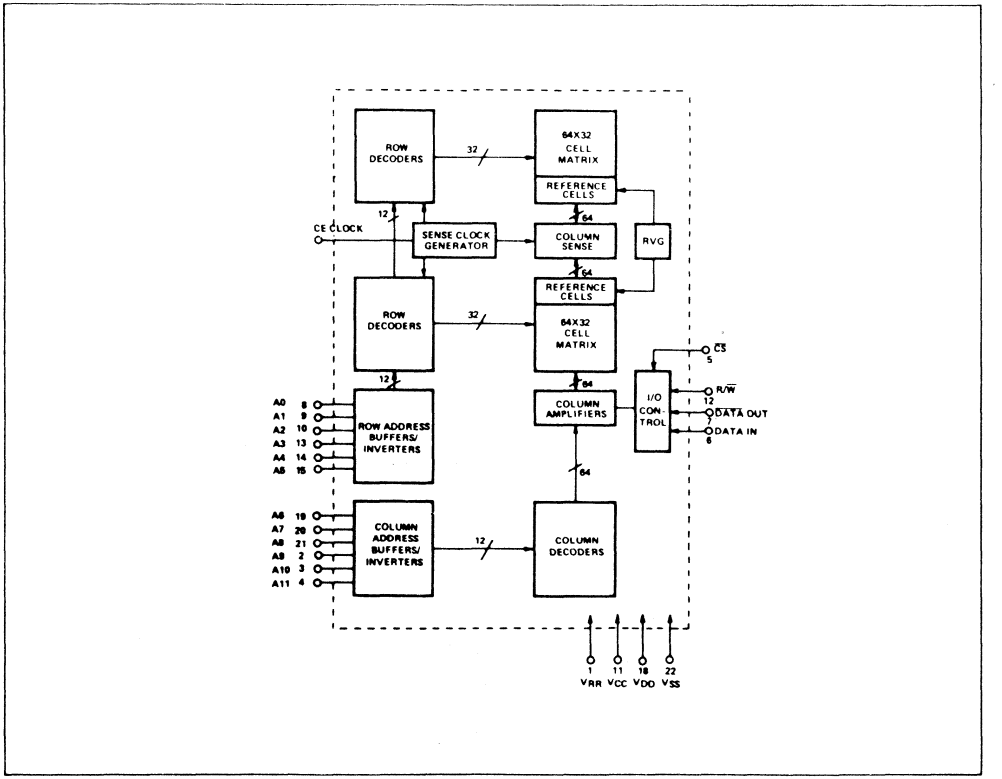
$\overline{\text{Data}}$ Out –

The output buffer is a totem-pole tri-state structure that will drive two standard TTL loads. The high impedance (disconnect) state occurs when Chip Enable is low or when the $\overline{\text{Chip Select}}$ input is high. When enabled, the output goes to a TTL "0" level before valid data appears. Output data is the complement of input data.

NOTES

1. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage larger than the rated maximum.
2. Typical values are at +25°C and nominal supply voltages.
3. Valid data is always preceded by a logic "0" output when the output buffers are enabled.
4. If CS goes low later than maximum t_{CSD}, data access time, and therefore cycle time, are increased accordingly.
5. If CS goes low after R/W goes low, t_{DS} is with respect to the falling edge of CS rather than R/W.
6. The internal write signal is a combination of CS and R/W. As a result, the internal write pulse width is a function of t_{WCH} as well as t_{WW}.
7. Depends on output loading. The V_{CC} supply is connected to the output buffer only.

BLOCK DIAGRAM



DC CHARACTERISTICS T_A = 0°C to 70°C, recommended supply voltage range (all voltages referenced to V_{SS})

PARAMETER		CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{IH}	Input high voltage (non-clock inputs)		2.2		V_{DD}	V
V_{IL}	Input low voltage (non-clock inputs)		-0.6		0.6	V
V_{CH}	Clock input high voltage		V_{DD}-1	V_{DD}	V_{DD}+1	V
V_{CL}	Clock input low voltage		-0.6		0.6	V
I_I	Input current (all inputs)	V_{IN} = +5 volts			10	μA
I_{LO}	Output leakage current	V_{OUT} = +5 volts, output disabled			10	μA
I_{BB}	V_{BB} supply current	V_{BB} = -5 volts, V_{DD} = 12 volts, V_{SS} = 0 volts			100	μA
I_{DD1}	V_{DD} supply current during CE clock high			40	60	mA
I_{DD2}	V_{DD} supply current during CE clock low			0.2	0.5	mA
I_{DD3}	Average V_{DD} supply current during t_{WC} or t_{RC}	t_{CE} = 320 ns, t_{WC} = t_{RC} = 470 ns		33		mA
I_{DD4}	Average V_{DD} supply current during t_{RMWC}	t_{CE} = 560 ns, t_{RMWC} = 710 ns		35		mA
I_{CC1}	V_{CC} supply current (operating)	Note 7				
I_{CC2}	V_{CC} supply current				100	μA
V_{OH}	Output high voltage	I_{OUT} = -2.0 mA	2.4		V_{CC}	V
V_{OL}	Output low voltage	I_{OUT} = 3.2 mA			0.4	V

RECOMMENDED SUPPLY VOLTAGES Measured with respect to V_{SS}

PARAMETER	LIMITS			
	MIN	TYP	MAX	UNIT
V_{DD}	11.4	12.0	12.6	V
V_{BB}	-4.5	-5.0	-5.5	V
V_{CC}	4.5	5	V_{DD}	V
V_{SS}		0.0		V

AC CHARACTERISTICS T_A = 0°C to 70°C, recommended supply voltage range

PARAMETER		CONDITIONS	MIN	TYP(2)	MAX	UNIT
t_{REF}	Time between refresh	T_A = 70°C			2	ms
C_{IN1}	Input capacitance (addresses and read/write)	V_{CL} = 0 V, V_{DD} = 12 V, V_{BB} = -5 V, V_{CC} = 5 V, f = 1 mHz		5	7	pF
C_{IN2}	Input capacitance (Chip select and data in)			4	6	pF
C_{OUT}	Output capacitance	V_{CL} = 0 V V_{DD} = 12 V		5	7	pF
C_{INC}	Clock input capacitance	V_{CH} = 12 V V_{BB} = -5 V		18	22	pF
		V_{CL} = 0 V V_{CC} = 5 V F = 1 mHz		23	27	pF

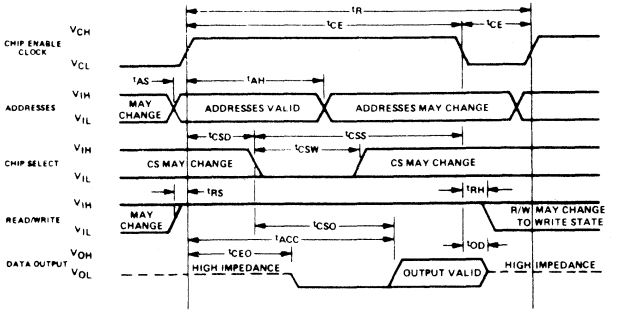
AC CHARACTERISTICS (Cont'd.)

PARAMETER		CONDITIONS	MIN	TYP (2)	MAX	UNIT
READ CYCLE						
t_R	Read cycle time		470			ns
t_{CE}	Chip enable pulse width		320			ns
$t_{\overline{CE}}$	$\overline{\text{Chip enable}}$ pulse width		150			ns
t_{AS}	Address set-up time		0			ns
t_{AH}	Address hold		150			ns
t_{CSS}	Chip select set-up time		240			ns
t_{CSW}	Chip select width		150			ns
t_{RS}	Read set-up time		0			ns
t_{RH}	Read hold time		40			ns
t_{CEO}	Chip enable to output enabled	Note 3		150		
t_{OD}	$\overline{\text{Chip enable}}$ to output disabled		10			ns
t_{ACC}	Chip enable to $\overline{\text{DATA}}$ valid				300	ns
t_{CSO}	Chip select to output delay				220	ns
t_{CSD}	Chip select delay from $\overline{CE}$ clock	Note 4			80	ns
WRITE CYCLE						
t_W	Write cycle time		470			ns
$t_{\overline{CE}}$	Chip enable pulse width		320			ns
$t_{\overline{CE}}$	Chip enable pulse width		150			ns
t_{AS}	Address to chip enable set-up time		0			ns
t_{AH}	Address hold time		150			ns
t_{CSS}	Chip select set-up time		240			ns
t_{CSW}	Chip select width		150			ns
t_{WS}	Write set-up time		240			ns
t_{WW}	Write pulse width		200			ns
t_{DS}	Data set-up time with respect to R/W	Note 5	0			ns
t_{DH}	Data hold time with respect to CE clock		40			ns
t_{WCH}	Write to chip select hold time	Note 6	200			ns

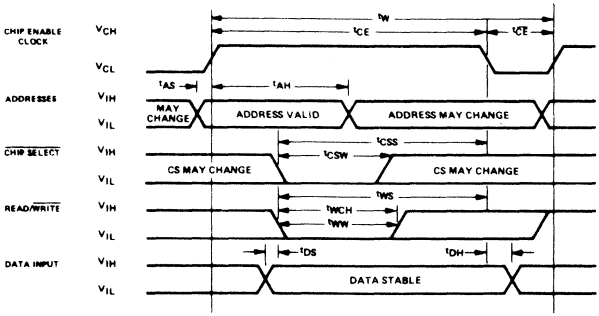
AC CHARACTERISTICS (Cont'd.)

PARAMETER		CONDITIONS	MIN	TYP (2)	MAX	UNIT
READ-MODIFY-WRITE CYCLE						
t_{RMW}	Read-modify-write cycle time		710			ns
t_{CE}	Chip enable clock pulse width		560			ns
$t_{\overline{CE}}$	Chip enable pulse width		150			ns
t_{AS}	Address to chip enable set-up time		0			ns
t_{AH}	Address hold time		150			ns
t_{CSS}	Chip select to write pulse set-up time		240			ns
t_{CS}	Chip select pulse width		150			ns
t_{RS}	Read to chip enable set-up time		0			ns
t_{RH}	Read to chip enable hold time		320			ns
t_{WW}	Write pulse width		200			ns
t_{WS}	Write set-up time		240			ns
t_{VW}	Previous data valid with respect to write pulse		50			ns
t_{CSD}	Chip select delay from CE clock	Note 4			80	ns
t_{DS}	Data set-up time with respect to write pulse		0			ns
t_{DH}	Data hold time with respect to CE clock		40			ns
t_{OD}	Chip enable to output disabled		10			ns
t_{CEO}	Chip enable to output enabled			150		ns
t_{ACC}	Chip enable to data valid				300	ns

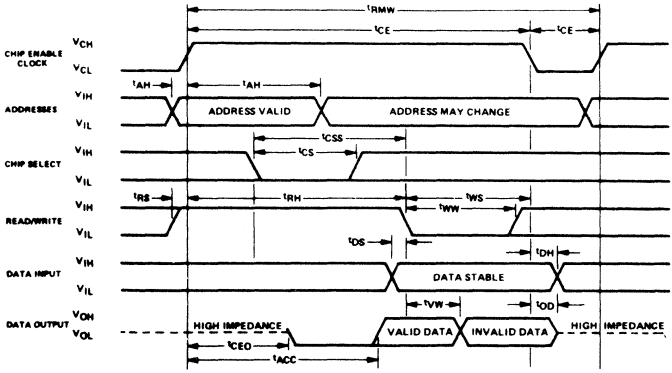
READ CYCLE TIMING



WRITE CYCLE TIMING



READ-MODIFY-WRITE CYCLE TIMING



INTERNAL OPERATION

The basic memory cell used in the 2604 consists of a single transistor and a storage capacitor (Q_1 and C_s, respectively, in Figure 1). Cells are organized in 64 rows and 64 columns. Individual rows are selected by decoding addresses A_0 through A_5 while the states of addresses A_6 through A_{11} determine which column is selected.

There is a differential sense amplifier for each column. These sense amplifiers are located in the center of the memory matrix. On each side of this row of sense amplifiers is a row of reference cells. As shown in Figure 2, a reference voltage generator is connected to the storage capacitor in each reference cell. When the Chip Enable clock is low, a voltage that is approximately halfway between a "1" level and a "0" level is directly written into the reference cell capacitors. At the same time, the voltage across the sense amplifier is reduced to zero through the device controlled by an internal clock signal, 0.

When Chip Enable goes high the addresses are gated into the 2604, and the decoders select one of 64 rows and one of 64 columns plus a reference row. The reference row that is selected is always on the opposite side of the sense amplifiers from the selected row. When a given data row is selected, all the cells on the row share their charge with the parasitic capacitance on its half of the respective columns. At the same time, the appropriate reference row shares its charge with the parasitic capacitance on its half of the respective columns. This charge sharing results in a particular voltage level on each column that is a function of the data stored in each cell in the selected row. This voltage is either higher or lower than that on the reference cell side of the sense amplifier, which resulted from the reference cell's sharing charge on its half of the column. This voltage difference is amplified and latched in the sense amplifier when 0_D, an internal clock signal, goes high. The resulting amplified logic level is then restored on the storage capacitors in the 64 cells on the selected row. This restoration is necessary since each cell shared its charge state with its column. The latched data on the selected column is then steered to the output buffer through the column switching matrix.

A write operation is performed in much the same manner except that the selected column is connected to the data input line. Then the sense amplifier is forced to latch according to the input data. All other cells on the selected row are refreshed during the write cycle.

FIGURE 1

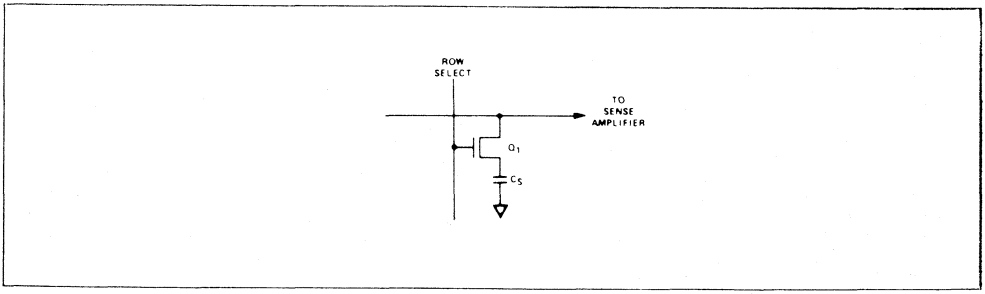
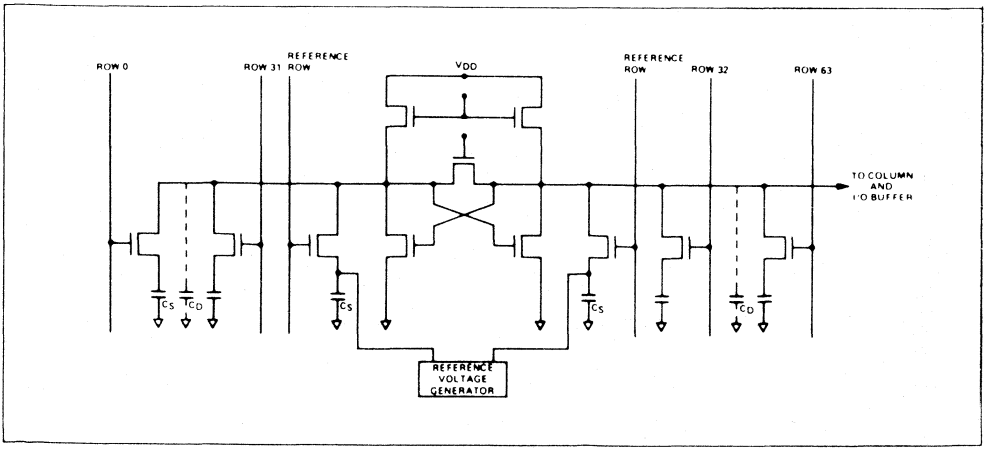


FIGURE 2



signetics ROM / PROM SELECTION GUIDE

Type		Confi-guration	Output	Signetics Part No.
TTL	ROM	256x4	OC TS	82S226 82S229
		512x4	OC TS	82S230 82S231
		256x8	TS	8204/S214
		512x8	TS	8205/S215
		1024x4	TTL	8228

Type		Org.	Output	Signetics Part No.
TTL	PROM	32x8	OC TS	82S23 82S123
		256x4	OC TS	82S126 82S129
		512x4	OC TS	82S130 82S131
		256x8	TS	82S114
		512x8	TS	82S115
	FPLA	16x48x8	TS OC	82S100 82S101
ECL	PROM	32x8	OE	10139
		256x4	OE	10149

Type		Org.	Max. Access Time (ns)	Signetics Part No.
MOS	ROM	64x8x5	600	2513
		64x6x8	600	2516
		64x9x9	700	2526
		512x8	700	2530
		2048x4	950	2580
		1024x8	650	2608

OC = Open Collector
TS = Tri-State
TTL = Totem Pole
OE = Open Emitter

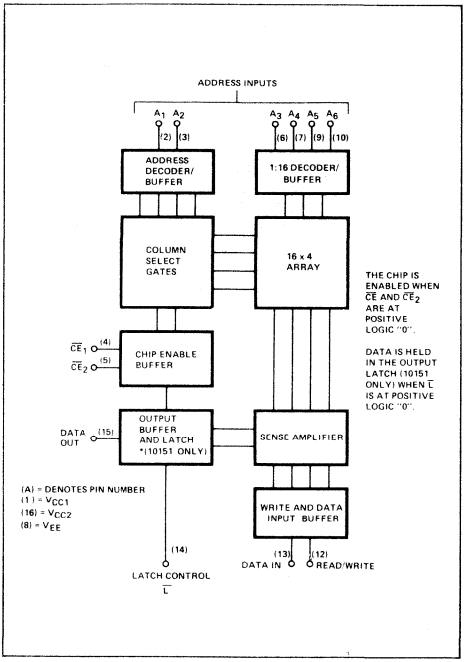
For further information on these devices request "SIGNETICS ROM/PROM BOOKLET" from your local Sales Office/Distributor.

DESCRIPTION

The 10140, 10148 and 10151 are 64 Bit ECL Random Access Memories (RAM's) organized as 64 words with 1 bit per word. The words are selected by six binary address lines; full word decoding is incorporated on the chip. Two chip enable input lines are provided for additional decoding flexibility. The chip is disabled when either chip enables are high, which causes the output of the 10140 and 10148 to go low.

The 10151 has an internal latch on the chip to provide the Write-While-Read capability. When the latch control line, $\overline{L}$ is a "1" and data is being read from the 10151 the latch is effectively bypassed. The data at the output will be that of the addressed word. When I goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When L goes from "0" to "1" the outputs unlatch and will take the state of the addressed word. The 10151 and 10148 logic levels are fully compatible with the 10,000 series and are specified for driving a 50Ω load. The 10140 is compatible with series 10,000 ECL except the output is specified for driving a 90Ω load.

LOGIC DIAGRAM



FEATURES

- 10 ns TYPICAL ACCESS TIME
- 16 PIN PACKAGE
- ON THE CHIP LATCH (AVAILABLE ON 10151)
- ON THE CHIP DECODING
- TWO CHIP ENABLE CONTROL LINES
- HIGH IMPEDANCE INPUTS 50k OHM PULL-DOWN
- OPEN EMITTER OUTPUTS

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
CONTROL STORE

TRUTH TABLE (10151)

$\overline{CE}$	$\overline{RW}$	$\overline{L}$	MODE	OUTPUTS
0	0	0	Write Data	
0	0	1	Write Data	
0	1	0	Read	Data stored in addressed word
0	1	1	Read	Data stored in addressed word
1	0	0	Chip Disabled	Data from last address when CE = "0"
1	0	1	Chip Disabled	Logical "1"
1	1	0	Chip Disabled	Data from last address when CE = "0"
1	1	1	Chip Disabled	Logical "1"

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{IL} min	Vdc
Output Source Current	I_o	40	mAdc
Storage Temperature Range	T_{stg}	-55 to +125	°C
Operating Junction Temperature	T_J	110	°C
Operating Temperature Range	T_A	-30 to +85	°C
Power Supply Regulation Required	—	±10% ±5%	—

$V_{CC1} = V_{CC2} = Gnd$

SWITCHING CHARACTERISTICS $T_A = 25°C$, $R_L = 50\Omega$ for 10148 and 10151, $R_L = 90\Omega$ for 10140

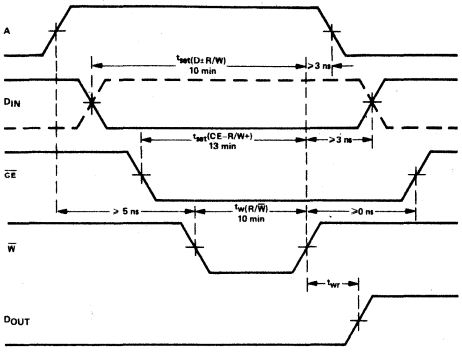
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Chip Enable					
Turn-On	t_{CE-D+}	—	8	12	ns
Turn-Off	t_{CE+D-}	—	8	12	
Access Time for Address to Output					
	t_{A+D+}	—	10	15	ns
	t_{A+D-}	—	10	15	
	t_{A-D+}	—	10	15	
	t_{A-D-}	—	10	15	
Write Pulse Width	$t_{w(R/W)}$	10			ns
Chip Enable Pulse Width	$t_{w(CE)}$	13			ns
Set-Up Time for Data to Write	$t_{set(D±R/W+)}$	10			ns
Set-Up Time for Data to Chip Enable	$t_{set(D±CE+)}$	10			ns
Set-Up Time for Write to Chip Enable	$t_{set(W-CE+)}$	10			ns
Set-Up Time for Chip Enable to Write	$t_{set(CE-R/W+)}$	13			ns
Set-Up Time for Data to Latch (10151 only)	$t_{set(D±I-)}$				ns
Set-Up Time for Latch Release to Data (10151 only)	$t_{set(I+D±)}$				ns
Set-Up Time for Latch to Address (10151 only)	$t_{set(I-A±)}$				ns

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $R_L = 50\Omega$ for 10148 and 10151, RL = 90Ω for 10140

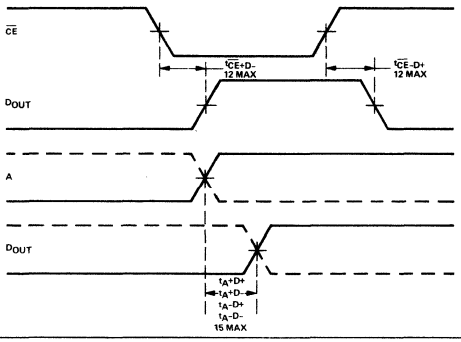
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Drain Current (V_{EE} = -5.2 V)	I_{EO}	—	80	—	mAdc
Input Current					μAdc
(V_{IH} = -0.810 V, V_{EE} = -5.2 V)	I_{inH}	—	—	265	
(V_{IL} = -1.850 V, V_{EE} = -5.2 V)	I_{inL}	0.5	—	—	
Output Voltage					
Logic "1" (V_{IH} = -0.810 V, V_{IL} = -1.850 V, V_{EE} = -5.2 V)	V_{OH}	-0.960	—	-0.810	Vdc
Logic "0" (V_{IH} = -0.810 V, V_{IL} = -1.850 V, V_{EE} = -5.2 V)	V_{OL}	-1.990	—	-1.650	Vdc
Threshold Voltage					
Logic "1" (V_{IHA} = -1.105 V, V_{ILA} = -1.475 V, V_{EE} = -5.2 V)	V_{OHA}	-0.980	—	—	Vdc
Logic "0" (V_{IHA} = -1.105 V, V_{ILA} = -1.475 V, V_{EE} = -5.2 V)	V_{OLA}	—	—	-1.630	Vdc

TIMING DIAGRAMS

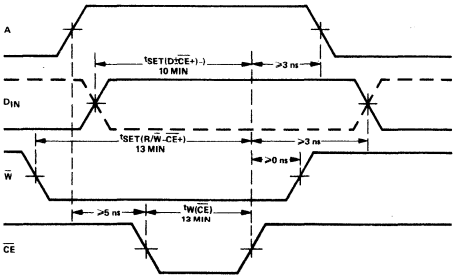
WRITE TIMING DIAGRAMS—WRITE STROBE MODE



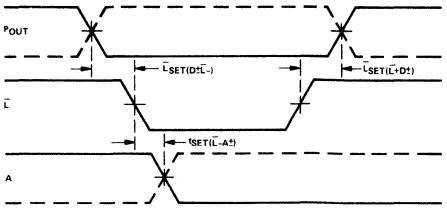
READ TIMING DIAGRAM



CHIP ENABLE STROBE MODE



10151 LATCH TIMING DIAGRAM



10145 F, I -30°C to +85°C

DIGITAL 10,000 ECL SERIES

DESCRIPTION

The 10145 is an ECL 64-bit read-write random access memory organized as 16 words of 4 bits each. Words are selected through fully decoded and buffered inputs when the chip enable ($\overline{CE}$) is low. Data is written into the selected word by bringing the READ/$\overline{WRITE}$ input low. Outputs are low during write.

On-chip input pulldown resistors allow any unused inputs to be left open. Open emitter outputs allow corresponding bits of different devices to be tied together to form a "Wire OR" logic connection.

The 10145 utilizes separate internal metal systems and wire bonds for V_{CC1} and V_{CC2}. The exceptionally high speed of the 10145 makes it particularly suited for register file and and scratch pad applications.

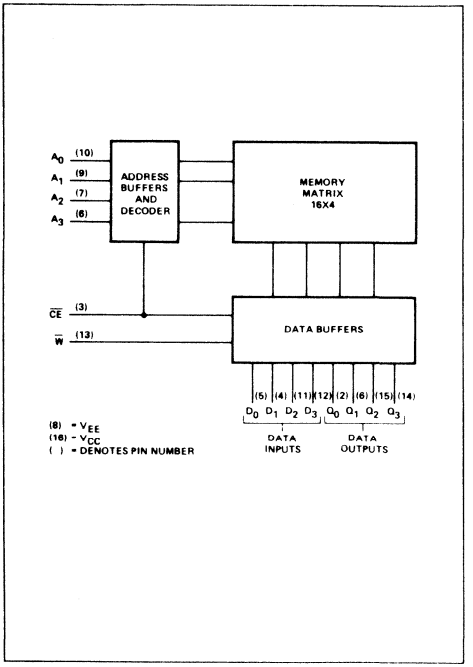
FEATURES

- 8.5ns ADDRESS ACCESS TIME (TYP)
- INPUT PULLDOWN RESISTORS
- OPEN EMITTER OUTPUTS AND CHIP ENABLE INPUT FOR MEMORY EXPANSION
- 50 Ohm OUTPUT SPECIFICATION
- SINGLE -5.2V POWER SUPPLY
- FULLY DECODED INPUTS
- FULLY COMPATIBLE WITH SIGNETICS 10,000 SERIES FAMILY OF INTEGRATED CIRCUITS

APPLICATIONS

SCRATCH PAD MEMORIES
BUFFER MEMORIES
REGISTER FILES
CONTROL STORES

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS V_{EE} = -5.2V, V_{CC} = 0V, R_L = 50Ω TO -2.0V

PARAMETER		TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
I_E	Supply Current		25°C		116	145	mA
I_{INH}	Input Current (Pins 3, 6, 7, 9, 10)	$V_{IN} = V_{IH}$ MAX.	25°C			200	μA
I_{INH}	Input Current (Pins 4, 5, 11, 12)	$V_{IN} = V_{IH}$ MAX.	25°C			220	μA
I_{INH}	Input Current (Pin 13)	$V_{IN} = V_{IH}$ MAX.	25°C			455	μA
I_{INL}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ MIN.	25°C	0.5			μA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
V_{OH}	Output Voltage	$V_{IN} = V_{IH}$ MAX., V_{IL} MIN.	-30°C 25°C 85°C	-1.06 -.96 -.89		-.89 -.81 -.70	Vdc
V_{OL}	Output Voltage	$V_{IN} = V_{IH}$ MAX., V_{IL} MIN.	-30°C 25°C 85°C	-1.89 -1.85 -1.825		-1.675 -1.65 -1.615	Vdc
V_{OHA}	Output Voltage (Threshold)	$V_{IN} = V_{IHA}, V_{ILA}$	-30°C 25°C 85°C	-1.08 -.98 -.91			Vdc
V_{OLA}	Output Voltage (Threshold)	$V_{IN} = V_{IHA}, V_{ILA}$	-30°C 25°C 85°C			-1.655 -1.63 -1.595	Vdc

SWITCHING CHARACTERISTICS V_{EE} = -3.2V, V_{CC} = 2V, R_L = 50Ω TO GND

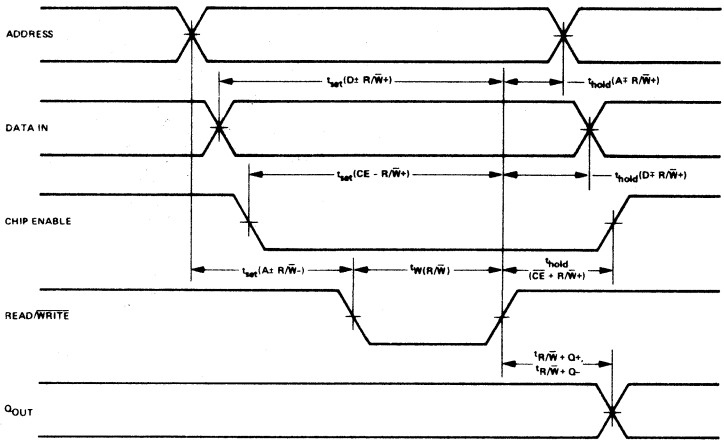
PARAMETER		MIN	TYP	MAX	UNITS
$t_{\overline{CE}} - Q+$, $t_{\overline{CE}} + Q-$	Access Time – Chip Enable to Output		5.0	7.5	ns
$t_A + Q+$, $t_A - Q+$	Address to Output		8.5	13.0	ns
$t_A + Q-$, $t_A - Q-$					
	Write Strobe Mode				
$t_{SET}(D\pm R/\overline{W}+)$	Data Set-up	11.0	7.5		ns
$t_{SET}(CE- R/\overline{W}+)$	Chip Enable Set-up	16.5	11.0		ns
$t_{SET}(A\pm R/\overline{W}-)$	Address	5.3	3.5		ns
$t_{HOLD}(D\mp R/\overline{W}+)$	Data Hold	4.5	3.0		ns
$t_{HOLD}(\overline{CE} + R/\overline{W}+)$	Chip Enable Hold	4.5	3.0		ns
$t_{HOLD}(A\mp R/\overline{W}+)$	Address Hold	5.3	3.5		ns
$t_{R/\overline{W}+} Q+$, $t_{R/\overline{W}+} Q-$	Recovery Time		7.5	11.0	ns
$t_{W(R/\overline{W})}$	Write Pulse Width	11.0	7.5		ns
	Chip Enable Strobe Mode				
$t_{SET}(D\pm \overline{CE}+)$	Data Set-up	11.0	7.5		ns
$t_{SET}(R/\overline{W}- \overline{CE}+)$	Read/Write Set-up	16.5	11.0		ns
$t_{SET}(A\pm\overline{CE}-)$	Address Set-up	4.5	3.0		ns
$t_{HOLD}(D\mp\overline{CE}+)$	Data Hold	4.5	3.0		ns
$t_{HOLD}(R/\overline{W} + \overline{CE} +)$	Read/Write Hold	4.5	3.0		ns
$t_{HOLD}(A\mp CE+)$	Address Hold	4.5	3.0		ns
$t_{W(\overline{CE})}$	Chip Enable Pulse Width	11.0	7.5		ns
t_+	Rise Time (20%–80%)	1.1	2.5	4.0	ns
t_-	Fall Time (20%–80%)	1.1	2.5	4.0	ns

TEST VOLTAGE VALUES
Vdc ± 1%

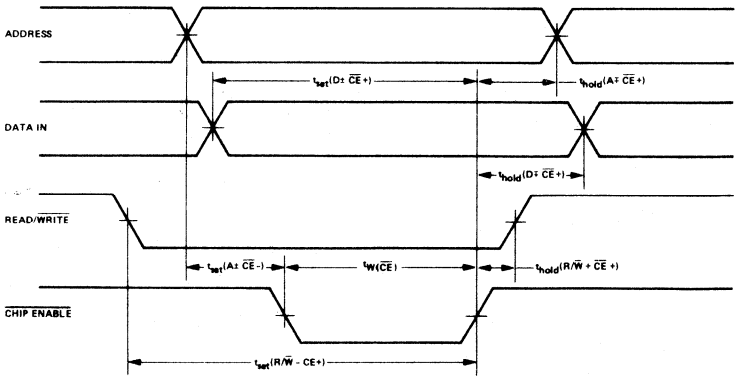
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

TIMING DIAGRAMS

WRITE CYCLE
READ/WRITE STROBE MODE

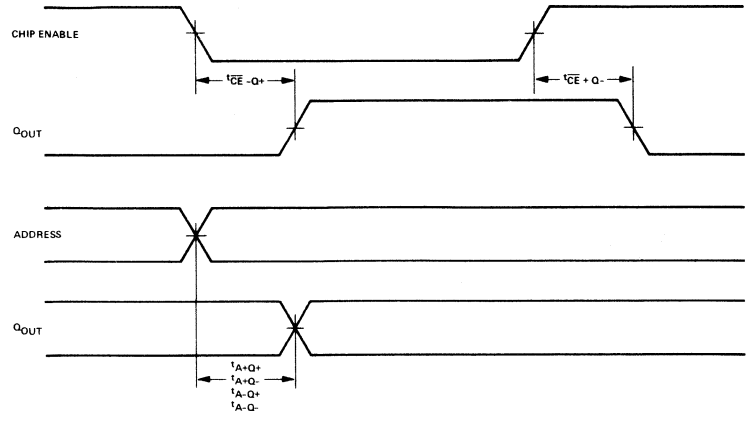


WRITE CYCLE
CHIP ENABLE STROBE MODE

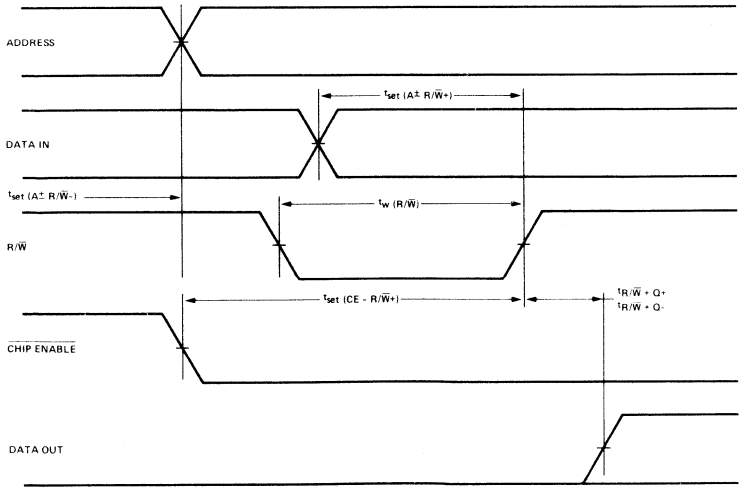


TIMING DIAGRAMS (Cont'd)

READ CYCLE



WRITE/READ CYCLE



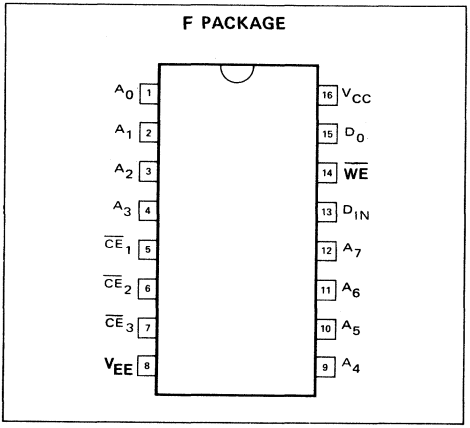
DESCRIPTION

The 10144 is an ECL 256-bit read-write random access memory organized as 256 words of 1 bit each. Words are selected through fully decoded and buffered inputs when the chip enable (CE) is low. Data is written into the selected word by bringing the READ/WRITE input low. Outputs are low during write.

On-chip input pulldown resistors allow any unused inputs to be left open. Open emitter outputs allow corresponding bits of different devices to be tied together to form a "Wire OR" logic connection.

The exceptionally high speed of the 10144 makes it particularly suited for register file and scratch pad applications.

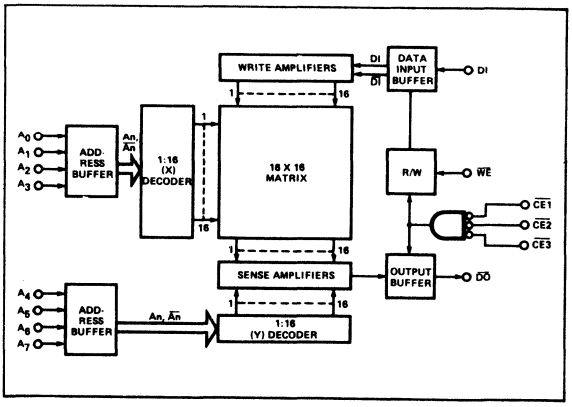
PIN CONFIGURATION



FEATURES

- 20ns ADDRESS ACCESS TIME (TYP)
- INPUT PULLDOWN RESISTORS
- OPEN EMITTER OUTPUTS AND CHIP ENABLE INPUT FOR MEMORY EXPANSION
- 50 Ohm OUTPUT SPECIFICATION
- SINGLE -5.2V POWER SUPPLY
- FULLY DECODED INPUTS
- FULLY COMPATIBLE WITH SIGNETICS 10,000 SERIES FAMILY OF INTEGRATED CIRCUITS

BLOCK DIAGRAM



APPLICATIONS

SCRATCH PAD MEMORIES
BUFFER MEMORIES
REGISTER FILES
CONTROL STORES

ELECTRICAL CHARACTERISTICS V_{EE}=-5.2V VCC =0V R_L=50Ω TO -2.0V T_A=25°C

			TEST LIMITS				
Characteristic	**Symbol**	**Conditions**		**Min.**	**Typ.**	**Max.**	**Units**
Supply Current	IEE	V_{in}=V_{IH}max, Vilmin (in any logic combination)			80	112	mA
Input Current	$I_{in}H$	Vin = VIH max				200	μA
Input Current	$I_{in}L$	Vin = VIL min		0.5			μA
High Output Voltage	VOH	Vin = VIH max, VIL min		-0.96		-0.81	Vdc
Low Output Voltage	VOL	Vin = VIH max VIL min		-1.85	-1.75	-1.65	
High Output (Threshold)	V_{OHA}	Vin = VIHA, VILA		-0.98			Vdc
Low Output (Threshold)	V_{OLA}	Vin = VIHA, VILA				-1.63	Vdc

Test Voltage Values (Volts)				Test Temperature
V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	
-0.890	-1.890	-1.205	-1.500	-30°C
-0.810	-1.850	-1.105	-1.475	25°C
-0.700	-1.825	-1.035	-1.440	+85°C

SWITCHING CHARACTERISTICS V_{EE}=-5.2V VCC =0V R_L=50Ω TO -2.0V T_A=25°C

Characteristic	See	Min.	Max.	Units
Chip Enable Access $T_{A\ (\overline{CE}\text{-}Q)}$	1		10	ns
Address Access $T_{A\ (A\text{-}Q)}$	2		30	ns
Write Cycle Time* (Total)	3		45	ns
Address Setup Time $T_{S(A\text{-}\overline{W})}$	3		10	ns
Write Pulse Width PW ($\overline{W}$)	3	4	22	ns
Address Hold Time $T_{H(\overline{W}\text{-}A)}$	3		10	ns
Chip Enable Setup $T_{S(\overline{CE}\text{-}\overline{W})}$	3		25	ns
Data Setup Time $T_{S(D\text{-}\overline{W})}$	3 4		25 25	ns ns
Chip Enable Hold $T_{H(\overline{W}\text{-}\overline{CE})}$	3		3	ns
Data Hold Time $T_{H(\overline{W}\text{-}D)}$	3		3	ns
Write Recovery $T_{R(\overline{W}\text{-}Q)}$	4		20	ns
Rise and Fall Time T_R T_F (20-80%)	—	1.1	4.0	ns
Write Disable Time T_D ($\overline{W}$-Q)	4	5	10	ns

*Write Cycle Time Equals Sum of T_S (A-W); PW (W); TH (W-A)

AC WAVEFORMS

Fig. 1 CHIP ENABLE ACCESS TIME

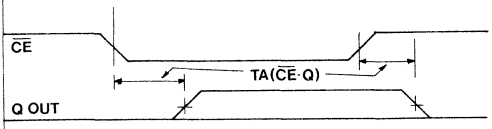


Fig. 2 ADDRESS ACCESS TIME

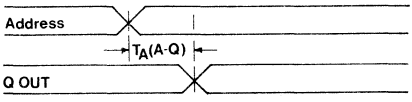


Fig. 3 MINIMUM WRITE CYCLE

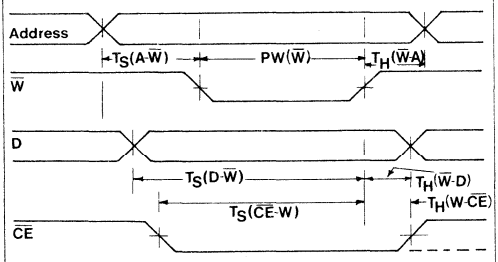
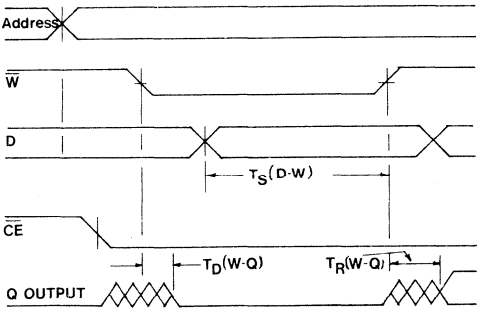


Fig. 4 SPECIAL WRITE CYCLE



DESCRIPTION

The 8220 CAM Element is a high speed monolithic array, incorporating the necessary addressing logic and eight identical memory cells organized as four words, each being two bits long. In reference to data-in/data-stored, the 8220 can be conditioned to perform the following functions: associate, write-in only, and read-out only.

When addressed into the "ASSOCIATE" mode, this element offers the novel capability of data association, where each cell (M_{nj}) will respond with a "Match" or "Mismatch" answer (Y_n) to each bit presented to the data inputs (I_j), depending on presence or absence of an alike bit stored within the cell.

Write-in can be simultaneously done to all bits, or one bit at a time. Read-out of stored information is performed on one word at a time. Cell-selection for read and write is performed by proper addressing of Y_n and A_n lines.

The element's output structures (Y_n and D_j) are of the "bare collector" variety and can be mutually connected, thus allowing direct expansion when multiple packages are employed. Expansion of the CAM may be implemented in both directions, i.e., in the word length and in the number of words.

The CAM circuit structure is the familiar TTL type (DCL Family) and fully compatible with TTL and DTL input/output structures.

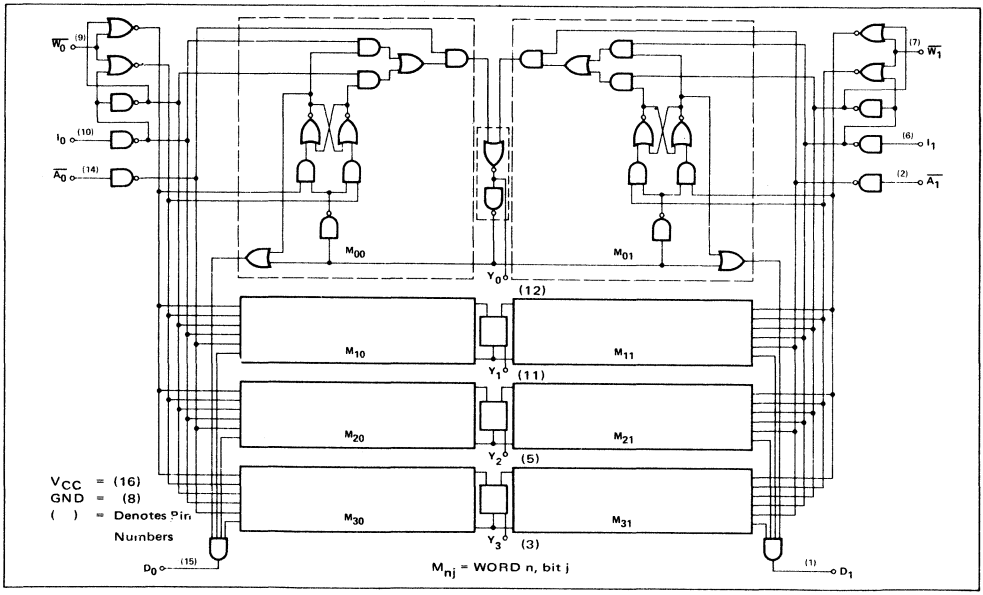
FEATURES

- WRITE ENABLE CONTROL LINES
- ASSOCIATE CONTROL LINES
- ADDRESS SELECT CONTROL LINES
- ASSOCIATES IN 20nsec TYP.
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)
- OPEN COLLECTOR OUTPUTS
- DIODE PROTECTED INPUTS

APPLICATIONS

DATA-TO-MEMORY COMPARISON
PATTERN RECOGNITION
HIGH SPEED INFORMATION RETRIEVAL
CACHE MEMORY
AUTO CORRELATION
VIRTUAL MEMORY
LEARNING MEMORY

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				$\overline{Wj}$	$\overline{Aj}$	I_j	Yi	Yk	Dj	NOTES
	MIN.	TYP.	MAX.	UNITS							
"0" Output Voltage											
Yn			0.4	V	2.0V	0.8V	2.0V	30mA			8, 9
			0.6	V	2.0V	0.8V	2.0V	60mA			
Dj			0.4	V	2.0V	2.0V			0.8V	20mA	8, 9
			0.6	V	2.0V	2.0V			0.8V	40mA	
"1" Output Leakage Current											
Yn			125	μA		2.0V					10
Dj			100	μA				0V	0V		10
"1" Input Current											
Ij and $\overline{A_j}$			40	μA		4.5V	4.5V				
$\overline{Wj}$			80	μA	4.5V						
"0" Input Current											
Ij, Yn and $\overline{Aj}$	-0.1		-1.2	mA		0.4V	0.4V	0.4V			
$\overline{W}_j$			-2.4	mA							
Power Consumption		85/ 425	118/ 590	mA/mW	V_{CC} = 5.0 Volts						

SWITCHING CHARACTERISTICS $0 \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				NOTES
	MIN.	TYP.	MAX.	UNITS	
Delay Time					
Associate (Aj to Yn)		20	35	ns	See Notes 8 & 11
Associate (Ij to Yn)		45	65	ns	See Notes 8 & 11
Read-Out (Yn to Dj)		30	45	ns	See Notes 8 & 11
Write-In to Read-Out (Wj to Dj)		45	65	ns	See Notes 8 & 11
Write Pulse Width	35	20		ns	See Notes 8 & 11
Ij Set-Up Time (I_{SO})	10			ns	See Notes 8 & 11
Ij Hold Time ($_{HO}$)	10			ns	See Notes 8 & 11

NOTES

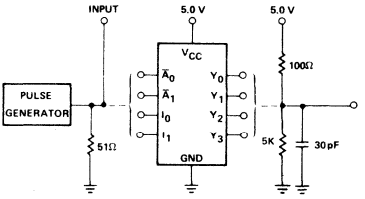
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Prior to this test write in a "0" in all or desired Memory cells as follows: Wj = Ij = 0V, Aj = V_{CC}.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Connect an external 1K ohm + 1% resistor from V_{CC} to the output terminal for this test.
11. See AC test Figures on the following pages.

MODE OF OPERATION

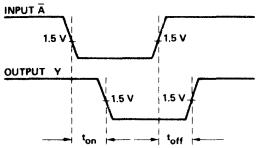
FUNCTION	$\overline{W_0}\ \overline{W_1}\ \overline{A_0}\ \overline{A_1}\ I_0\ I_1$	REMARKS (Ref. Definitions & Glossary)	FUNCTION	$\overline{W_0}\ \overline{W_1}\ \overline{A_0}\ \overline{A_1}\ I_0\ I_1$	REMARKS (Ref. Definitions & Glossary)
HOLD	1 1 1 1 x x	NO OPERATION	HOLD	1 1 1 1 x x	NO OPERATION
ASSOCIATE	1 1 1 0 x x	Question: $I_1 = M_{i1}$? Answer: YES — Y_i=1, Y_k=0; NO — $Y_i = Y_k$=0	WRITE-IN	1 0 1 1 x x	Forced Y_i=1, Y_k=0: WRITE I_1 into M_{i1}
				0 1 1 1 x x	Forced Y_i=1, Y_k=0: WRITE I_0 into M_{i0}
	1 1 0 1 x x	Question: $I_0 = M_{i0}$? Answer: YES — Y_i=1, Y_k=0; NO — $Y_i = Y_k$=0		0 0 1 1 x x	Forced Y_i=1, Y_k=0: WRITE I_1 and I_0 into M_{i1} and M_{i0}
			READ-OUT	1 1 1 1 x x	Forced Y_i=1, Y_k=0: D_0 = 1 - IF M_{i0}=1; 0 - IF M_{i0}=0
	1 1 0 0 x x	Question: $I_1 = M_{i1}$ and $I_0 = M_{i0}$? Answer: YES — Y_i=1, Y_k=0; NO — $Y_i = Y_k$=0		1 1 1 1 x x	Forced Y_i=1, Y_k=0: D_1 = 1 - IF M_{i1}=1; 0 - IF M_{i1}=0
				1 1 1 1 x x	Forced Y_i=0, Y_k=0: $D_0 = D_1$ = 1

AC TEST FIGURES AND WAVEFORMS

ASSOCIATE DELAY AND INPUT DELAY

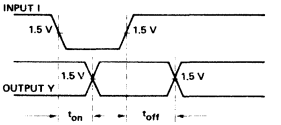


ASSOCIATE DELAY



NOTES:
1. When checking $\overline{A_0}$ let $\overline{A_1}$ = "1" and when checking $\overline{A_1}$ let $\overline{A_0}$ = "1".
2. $\overline{W_0} = \overline{W_1}$ = "1".

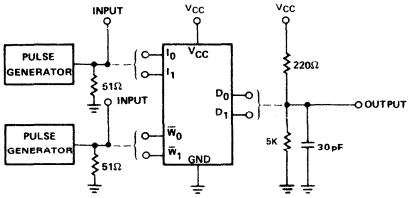
INPUT DELAY

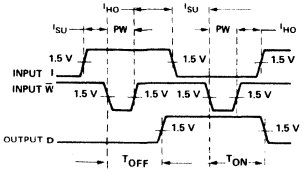


NOTES:
1. When checking I_1, $\overline{A_1}$ = "0" and $\overline{A_0}$ = "1" and when checking I_0, $\overline{A_0}$ = "0" and $\overline{A_1}$ = "1"
2. $\overline{W_0} = \overline{W_1}$ = "1".

AC TEST FIGURES AND WAVEFORMS (Cont'd)

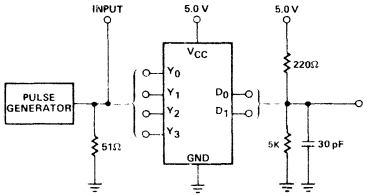
WRITE DELAY

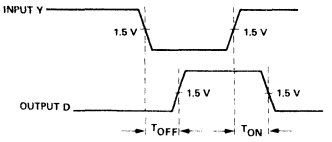




NOTES:
1. $A_0 = \overline{A}_1 = "1"$.
2. Let all non-selected Y's = "0".
3. W's pulse width is 40ns @50% points.

READ DELAY





NOTES:
1. A tested bit must store a "0".
2. $\overline{W}_0 = \overline{W}_1 = "1"$.
3. $\overline{A}_0 = \overline{A}_1 = "1"$.
4. All non-tested Y's = "0".

GENERAL NOTES FOR AC TESTING:
1. Use 5k Probes for all AC tests TEK 169 or equivalent.
2. The Pulse Generator signal should consist of the following
   Frequency: 10 MHz ±5 MHz
   Amplitude: 0V to 3V
   Rise & Fall Times: 5 ns ±2ns
3. i = bit number (i = 0, 1). j = word number (j = 0, 1, 2, 3).

INPUT/OUTPUT DEFINITIONS

I_j – Data Inputs
Data entering these terminals are either compared with stored information at the cell(s) in the "associate" mode or stored in the cell(s) in the "write-in" mode.

$\overline{A}_j$ – Associate Controls
A logical "0" at this pin enables Data-Cell association to result into a defined logical level at the Y_n lines (e.g. Y_n = "1" = Match, Y_n = "0" Mismatch). A logical "1" at this pin forces all Y_n to a "1".

$\overline{W}_j$ – Write Enable
A logical "0" at this control pin opens the gates of the selected word, allowing data-in to be stored. A logical "1" locks the gates such that data-in can no longer disturb the cell(s).

Y_n – "Associate" Output and Address Selection Control
During "Associate" mode these "bare collector" lines provide output results of match or mismatch between input and stored data (logical "1" = Match, logical "0" = Mismatch).

In the read and write modes these terminals act as input controls and word-select lines Y lines (Y_1) associated with words desired to accept writing of data or read-out are to be kept in the logical "1" state and the remaining Y lines (Y_k) to be forced to a logical "0" state. (Note that A = 1 forces all Y_n = 1).

D_j – Data Output
These are "bare collector" output lines indicating the state of one or more selected cells. Cell-Selection is accomplished as defined under "Y_n" above.

GLOSSARY OF TERMS - SUBSCRIPTS

A. n = Word number = 0, 1, 2 and 3
   j = Bit number = 0 or 1
   i = Input/Output number(s) associated with cell(s) upon which a "Write-in", "Read-out" or other function is being performed.
   k = Input/Output number(s) other than "i" above.
   M = Designation of Memory Cell (word) = eight identical cells in each package.

B. Examples
1. I_j for bit "1" equals I_1.
2. $M_{nj} = M_{10}$ = word "1" bit "0".
3. Y_i = 0, Y_k = 1: for i = words 1 and 3; then k = words 0 and 2: $Y_{1,3}$ = 0 and $Y_{0,2}$ = 1.

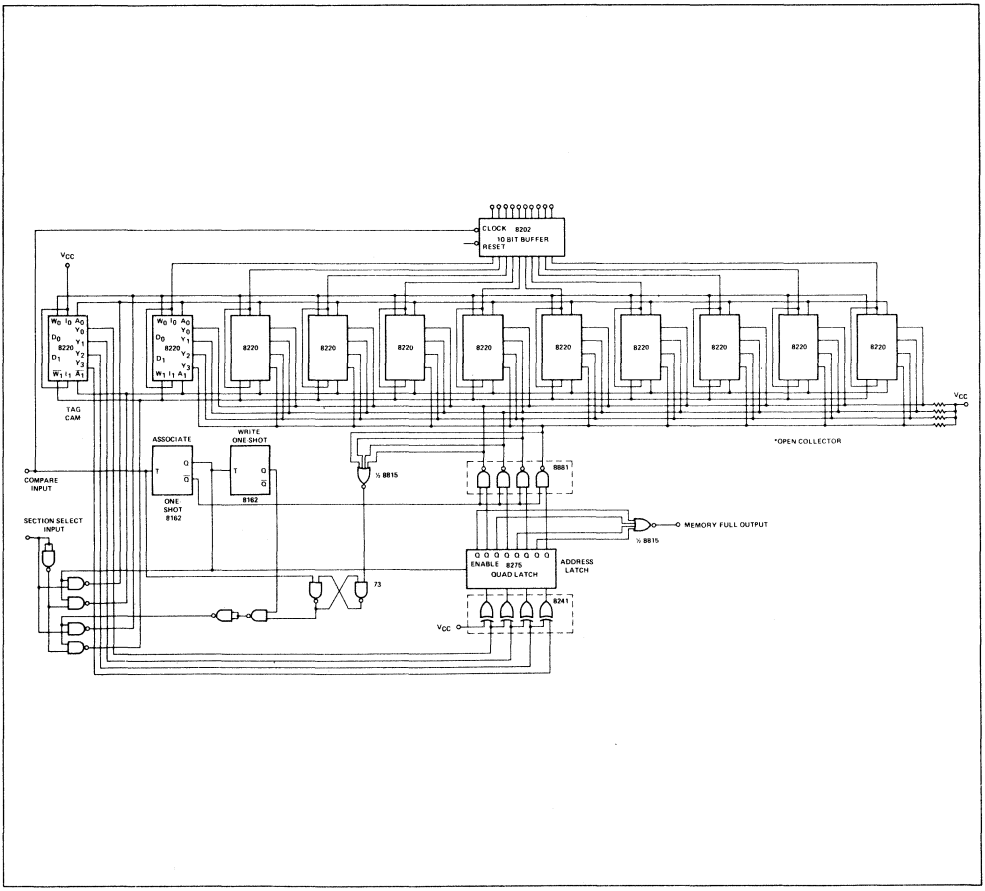
APPLICATION: LEARNING MEMORY

This system is a CAM array with peripheral IC circuitry designed to operate as a learning memory. It is organized in two sections of equal capacity, the total memory size (both sections) being 8 ten bit words. Either section can be selected through the section SELECT line, and the memory is easily expandable in the number of words and in word length.

By activating the COMPARE line, a new word is loaded into the buffer and is presented to the memory. Through the novel feature of data association, which is unique with CAM elements, the buffer's content is compared with the words stored in memory. If the input word, with which the memory was presented, is already contained in storage, no need for "learning" i.e. data acquisition, exists. This fact is indicated by a match from one of the Y_n lines ($Y_i = 1$) and thus no write command is initiated.

Before a WRITE operation is initiated, a location select has to be made such that the word to be written into the memory will go to the proper place. For this reason, a tag CAM is employed to keep track of memory locations, both empty and full. When a word is written into memory, a "1" is simultaneously written into the tag CAM. Thus, it is possible to keep track of the filled memory locations.

By monitoring the Y_n lines of the tag CAM, a convenient way of decoding an available address exists. Here exclusive OR circuitry is used which ensures that memory locations are filled successively when the need for "learning" exists. The quad latch is enabled before the write command is available to the CAM array. Thus the Y lines of unavailable memory locations are forced low ($Y_k = 0$).



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64-BIT BIPOLAR HIGH SPEED WRITE-WHILE-READ RAM (32x2 RAM)

82S21

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S21 is a TTL 64 bit Write-While-Read Random Access Memory organized in 32 words of 2 bits each. The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5 input decoder when the Read-Write enable input, CE is at logic "1". $\overline{W_0}$ and $\overline{W_1}$ are the write inputs for bit 0 and bit 1 of the word selected. $\overline{C}$ is the write control input. When $\overline{W_X}$ and $\overline{C}$ are both at logic "0" data on the I_0 and I_1 data lines are written into the addressed word. The read function is enabled when either $\overline{W_X}$ or $\overline{C}$ is at logic "1".

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, $\overline{L}$, is logic "1" and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When $\overline{L}$ goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When $\overline{L}$ goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

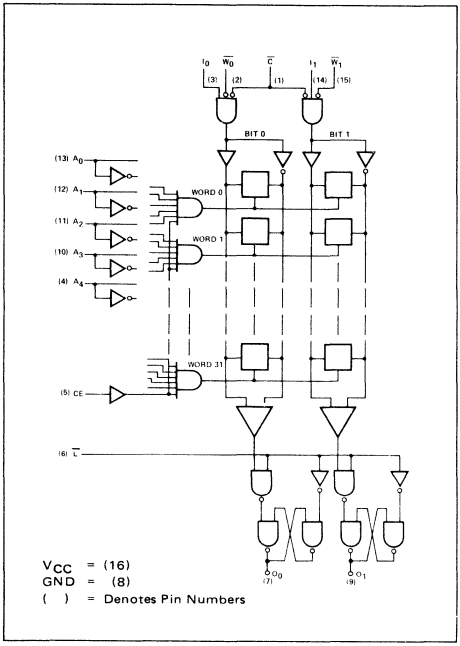
FEATURES

- **BUFFERED ADDRESS LINES**
- **ON CHIP LATCHES**
- **ON CHIP DECODING**
- **BIT MASKING CONTROL LINES**
- **ENABLE CONTROL LINE**
- **OPEN COLLECTOR OUTPUTS WITH 40mA CAPABILITY**
- **PROTECTED INPUTS**
- **VERY HIGH SPEEDS (25ns TYP)**

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
CONTROL STORE

LOGIC DIAGRAM



TRUTH TABLE

CE	$\overline{C}$	$\overline{W_0}$	$\overline{W_1}$	$\overline{L}$	Mode	Outputs
X	X	X	X	0	Output Hold	Data from last addressed word when CE = "1"
0	X	X	X	1	Read & Write Disabled	Disabled logic "1"
1	1	X	X	X	Read	Data stored in addressed word
1	0	1	1	X	Read	Data stored in addressed word
1	0	0	0	0	Write Data	Data from last word address when L went from "1" to "0"
1	0	0	0	1	Write Data	Data being written into memory
1	0	0	1	X	Write Data into Bit 0 Only	If $\overline{L}$ = 0: Data from last word address when L went from "1" to "0"
1	0	1	0	X	Write Data into Bit 1 Only	If $\overline{L}$ = 1: Data being written into the selected bit location and stored in other addressed location

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C; 4.75V \leq V_{CC} \leq 5.25$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			.45	V	V_{out} = 40mA	
"1" Output Leakage Current			40	μA	V_{out} = 5.5V	
"0" Input Current (All Inputs)			−1.6	mA	V_{in} = 0.45V	
"1" Input Current (All Inputs)			25	μA	V_{in} = 5.5V	
Input "0" Threshold Voltage			0.85	V		
Input "1" Threshold Voltage	2.0			V		
Power Consumption			130/683	mA/mW		
Input Clamp Voltage	−1.2				I_{in} = −18mA	

SWITCHING CHARACTERISTICS $0 \leq T_A \leq 75°C, 4.75 \leq V_{CC} \leq 5.25V$

CHARACTERISTICS		LIMITS				TEST CONDITIONS	NOTES
		MIN.	TYP.	MAX.	UNITS		
Read Access Time Address to Output	t_1		25	50	ns		
Address Set-Up Time	t_2	15	8		ns		
Data Set-Up Time	t_3	20	15		ns		
Address Hold Time	t_4	0			ns		
Control or Write Pulse Width	t_5	20	15		ns		
Write Access Time	t_6		20	25	ns		
Address to Latch Set-Up Time	t_7		25	50	ns		
Latch Address to Address Hold Time	t_8	10	7		ns		
Delatch Access Time	t_9		15	25	ns		
Data Hold Time Earliest	t_{10}	5	0		ns		

AC WAVEFORM

Read Access Time

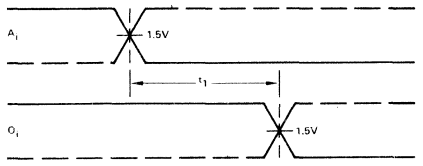
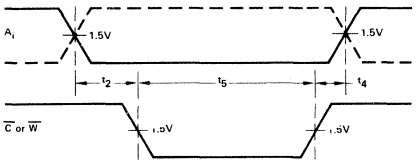


FIGURE 1

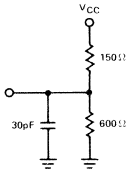
Address Setup and Hold Time



$t_r = t_f \leq 5$ ns, INPUT VOLTAGE = 2.8 Volts

FIGURE 2

TEST LOAD



AC WAVEFORMS

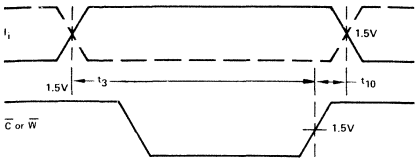


Fig. 3 Data Setup and Hold Time

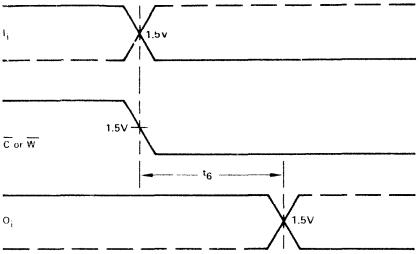


Fig. 4 Write Access Time

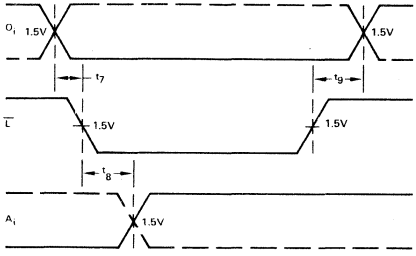
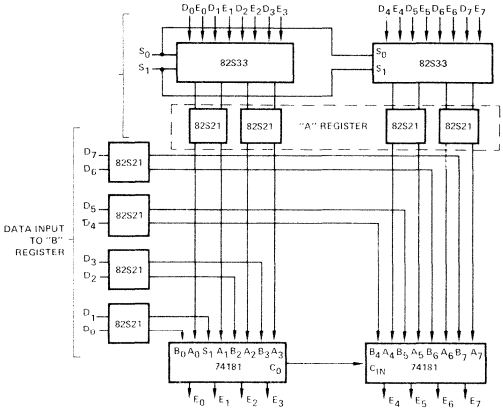


Fig. 5 Latch Times

TYPICAL APPLICATION



BASIC 8 BIT FULLY BUFFERED ACCUMULATOR

By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32 x 8 RAM register. Data is loaded directly into the "B" register. With this arrangement, the function A+B → A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.

signetics

HIGH-SPEED MULTIPORT MEMORY (8x4 MULTIPORT RAM)

82S12 82S112

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S12/112 is a Schottky TTL 32 bit multiport memory organized in 8 words of 4 bits each. The device is ideally suited for high speed accumulators and buffer memories.

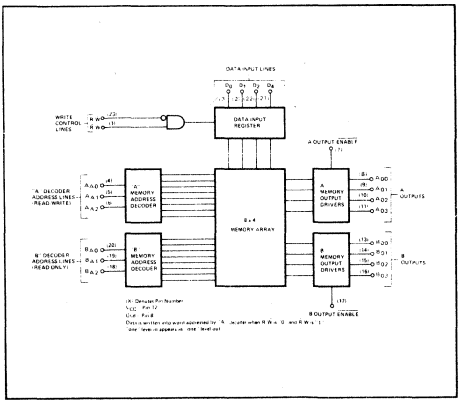
Stored data is addressed through 2 independent sets of 3-input decoders, and read out when the corresponding output enable line is low. Two separate word locations can, therefore, be read at the same time by enabling both the A and B output drivers. In addition, data can be read and written at the same time by utilizing the "A" address to specify the location of the word to be written, and the "B" address to specify the word to be read.

The 82S12/112 can be used in larger memory arrays since it includes all the control logic required to disable the chip and the outputs are open-collector devices suitable for "Wire-ORing."

FEATURES

- **LOW CURRENT INPUT BUFFERS (–25μA TYPICAL)**
- **SEPARATE INPUT DECODERS FOR EACH WORD**
- **SEPARATE OUTPUT ENABLE LINES FOR EACH WORD**
- **OPEN COLLECTOR (82S12) OR TRI-STATE (82S112) OUTPUTS**
- **2 WRITE ENABLE LINES**
- **FAST ACCESS (20 ns TYPICAL)**
- **USEFUL 8 X 4 ORGANIZATION**
- **TTL COMPATIBLE**
- **NON INVERTING DATA LINES**

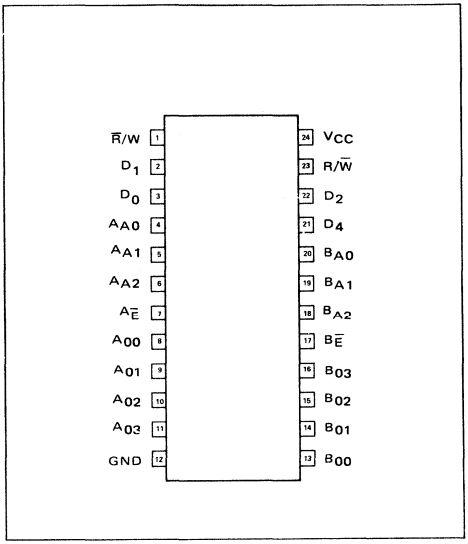
BLOCK DIAGRAM



APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
GENERAL REGISTER

PIN CONFIGURATION



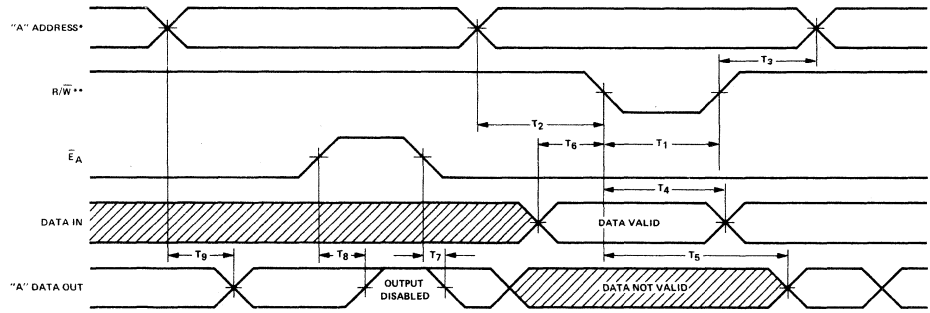
TRUTH TABLE

R/W	R/W	A OUTPUT ENABLE	B OUTPUT ENABLE	MODE	OUTPUTS A	OUTPUTS B
0	X	1	1	Outputs Disabled	"1"	"1"
0	X	1	0	Read	"1"	Data
0	X	0	1	Read	Data	"1"
0	X	0	0	Read	Data	Data
1	1	1	1	Read	"1"	"1"
1	1	1	0	Read	"1"	Data
1	1	0	1	Read	Data	"1"
1	1	0	0	Read	Data	Data
1	0	1	1	Write	"1"	"1"
1	0	1	0	Write	"1"	Data "B" Address
1	0	0	1	Write	Data Being Written	"1"
1	0	0	0	Write	Data Being Written	Data "B" Address

OBJECTIVE ELECTRICAL SPECIFICATIONS $0°C \leq T_A \leq 75°C; -4.75\ V \leq V_{CC} \leq 5.25\ V.$

CHARACTERISTICS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
Input "0" Current				−250	μA	$V_{in} = 0.45\ V$
Input "1" Current				25	μA	$V_{in} = 5.5\ V$
Input "0" Threshold Voltage				0.85	V	
Input "1" Threshold Voltage		2.0			V	
Input Clamp Voltage		−1.2			V	$I_{in} = -18\ mA$
Output "0" Current		16			mA	$V_{out} = 0.5\ V$
Output "0" Current		9.6				$V_{out} = 0.45\ V$
Output "1" Voltage (825112)		2.6			Volts	$I_{out} = -3.2\ mA$
Output Off Current (82S12)				40	μA	$V_{out} \leq 5.5\ V$
Output Off Current (82S112)		−40		+40	μA	$0.45 \leq V_{out} \leq 5.5\ V$
Power Consumption			110/550	160/840	mA/mW	Outputs Enabled
Write Pulse Width	T_1	30	15		ns	$T_A = 25°C$ Only
	T_1	45				
Address Set Up Time	T_2		10		ns	
Address Hold Time	T_3		0		ns	
Data Input Hold Time	T_4		0		ns	
Write Access Time	T_5		30		ns	
Data Input Set Up Time	T_6		5		ns	
Output Enable Time	T_7		10	20	ns	
Output Disable Time	T_8		10	20	ns	
Address Access Time	T_9		20	30	ns	

TIMING DIAGRAM



T_1 WRITE PULSE WIDTH – Width of write pulse (when R/W="1" and R/W="0")

T_2 ADDRESS SETUP TIME – Required delay between beginning of valid Address and beginning of Write pulse.

T_3 ADDRESS HOLD TIME – Required delay between end of Write pulse and end of valid Address.

T_4 DATA INPUT HOLD TIME – Required delay between start of Write pulse and end of Valid Data input.

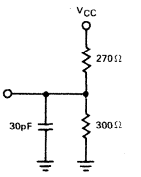
T_5 WRITE ACCESS TIME – Delay between beginning of Write pulse and Data Out at new value.

T_6 DATA INPUT SET-UP TIME – Required delay between beginning ov Valid Data Input and start of Write pulse.

T_7 OUTPUT ENABLE TIME – Delay between beginning of Output Enable high and when Data Output becomes valid.

T_8 OUTPUT DISABLE TIME – Delay between when Output Enable becomes low and Data Output is in off state.

T_9 ADDRESS ACCESS TIME – Delay between beginning of Valid Address (with Output Enable high, R/W high and R/W low) and when Data Output becomes valid.



A, C. LOAD

NOTES

*"B" Address functions identically in read mode. No write mode through B address decoder.

**R/W input is either the reverse of R/W or held high.

Outputs can be disabled during write cycle to penetrate a known output state during write.

DYNAMIC SHIFT REGISTER RANGE

Part Number	Capacity	Output Structure	On Chip Re-Circulate	Package No. of Leads	TYP Speed	Number of Clocks	Clock TTL Compati-bility	Power Supplies
2504	1024 BITS	Bare Drain	NO	TA-8, V-8	10.0 MHz	TWO	NO	+5, -5
2512	1024 BITS	Bare Drain	YES	K-10	3.0 MHz	TWO	NO	+5, -5
2525	1024 BITS	Bare Drain	YES	V-8	5.0 MHz	TWO	NO	+5, -5
2503	Dual 512 BITS	Bare Drain	NO	TA-8, V-8	10.0 MHz	TWO	NO	+5, -5
2505	512 BITS	Bare Drain	YES	K-10	3.0 MHz	TWO	NO	+5, -5
2524	512 BITS	Bare Drain	YES	V-8 q	5.0 MHz	TWO	NO	+5, -5
2502	Quad 256 BITS	Bare Drain	NO	B-16	10.0 MHz	TWO	NO	+5, -5
2506	Dual 100 BITS	Bare Drain	NO	T-8, V-8	4.0 MHz	TWO	NO	+5, -5
2507	Dual 100 BITS	7.5K PD	NO	T-8, V-8	4.0 MHz	TWO	NO	+5, -5
2517	Dual 100 BITS	20K PD	NO	T-8, V-8	4.0 MHz	TWO	NO	+5, -5

STATIC SHIFT REGISTER RANGE

Part Number	Capacity	Output Structure	On Chip Re-Circulate	Package No. of Leads	TYP Speed	Number of Clocks	Clock TTL Compati-bility	Power Supplies
2533	1024 BITS	Push Pull	JUMPER	V-8	2.0 MHz	ONE	YES	+5, -12
2527	Dual 256 BITS	Push Pull	YES	V-8	3.0 MHz	ONE	YES	+5, -12
2528	Dual 250 BITS	Push Pull	YES	V-8	3.0 MHz	ONE	YES	+5, -12
2529	Dual 240 BITS	Push Pull	YES	V-8	3.0 MHz	ONE	YES	+5, -12
2511	Dual 200 BITS	Tri-state	YES	A-14, K-10	3.0 MHz	ONE	YES	+5, -5, -12
2522	Dual 132 BITS	Push Pull	YES	V-8	3.0 MHz	ONE	YES	+5, -12
2521	Dual 128 BITS	Push Pull	YES	V-8	3.0 MHz	ONE	YES	+5, -12
2510	Dual 100 BITS	Tri-state	YES	A-14, K-10	3.0 MHz	ONE	YES	+5, -5, -12
2532	Quad 80 BITS	Push Pull	YES	B-16	3.0 MHz	ONE	YES	+5, -12
2509	Dual 50 BITS	Tri-state	YES	A-14, K-10	3.0 MHz	ONE	YES	+5, -5, -12
2519	Hex 40 BITS	Bare Drain	YES	B-16	3.0 MHz	ONE	YES	+5, -12
2518	Hex 32 BITS	Bare Drain	YES	B-16	3.0 MHz	ONE	YES	+5, -12

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